A New Paradigm in High-Speed and High-Efficiency Silicon Photodiodes for Communication—Part II: Device and VLSI Integration Challenges for Low-Dimensional Structures

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***Abstract*— The ability to monolithically integrate high-speed photodetectors (PDs) with silicon (Si) can contribute to drastic reduction in cost. Such PDs are envisioned to be integral parts of high-speed optical interconnects in the future intrachip, chip-to-chip, board-to-board, rack-to-rack, and intra-/interdata center links. Si-based PDs are of special interest since they present the potential for monolithic integration with CMOS and BiCMOS very-large-scale integration and ultralarge-scale integration electronics. In the second part of this review, we present the efforts pursued by the researchers in engineering and integrating Si, SiGe alloys, and Ge PDs to CMOS and BiCMOS electronics and compare the performance of recently demonstrated CMOS-compatible ultrafast surface-illuminated Si PD with absorption-enhancing low-dimensional structures. We discuss the advantages and challenges of device design with micro-/nanostructures, and finally, we conclude with the future directions that low-dimensional structures can offer to potentially cause a paradigm shift in high-performance PD design for various applications such as extended-reach links, single-photon detection, light detection and ranging, and high-performance computing.**

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***Index Terms*— CMOS integration, extended-reach links, high speed, high-efficiency photodetectors (PDs), high-performance computing, light detection and ranging, micro-/nanostructures, single-photon detection, surface states, very-large-scale integration (VLSI) and ultralarge-scale integration (ULSI).**

I. Introduction

THE rise of distributed computing, cloud storage, social media, and affordable hand-held devices currently allow extreme ease of transferring a plethora of data including videos, pictures, and texts, all over the world. We are only at the beginning of a new era that promises unprecedented quality of life in a healthier, more secure, highly connected and efficient way. Autonomous vehicles, smart houses with smart appliances, and intelligent infrastructures will be the norms of future living. Networking of these devices, namely, Internet of Things (IoTs) will bring along big data that needs to be transmitted, stored, and analyzed in more efficient and secure ways [1]. Thus, the transformation of the current data centers is inevitable to meet these demands. Either building many mini data centers or scaling up the existing ones will require technology development for high-capacity network data transmission (Fig. 1). The enormous number of connections with low latency will require receivers with high-bandwidth and high-efficiency together along with minimal power consumption. To keep up with demand in the data traffic, current copper wire interconnects utilized in data centers need to be fully replaced by fast and low-cost optical fiber interconnects [2], [3]. Fig. 2 shows the target cost range for optical interconnects for several stages of connections at the data centers [3]. The development of low-cost very-large-scale integration (VLSI)-CMOS compatible devices and components are crucial and high-efficiency and high-speed photodetectors (PDs) are among the most critical devices.

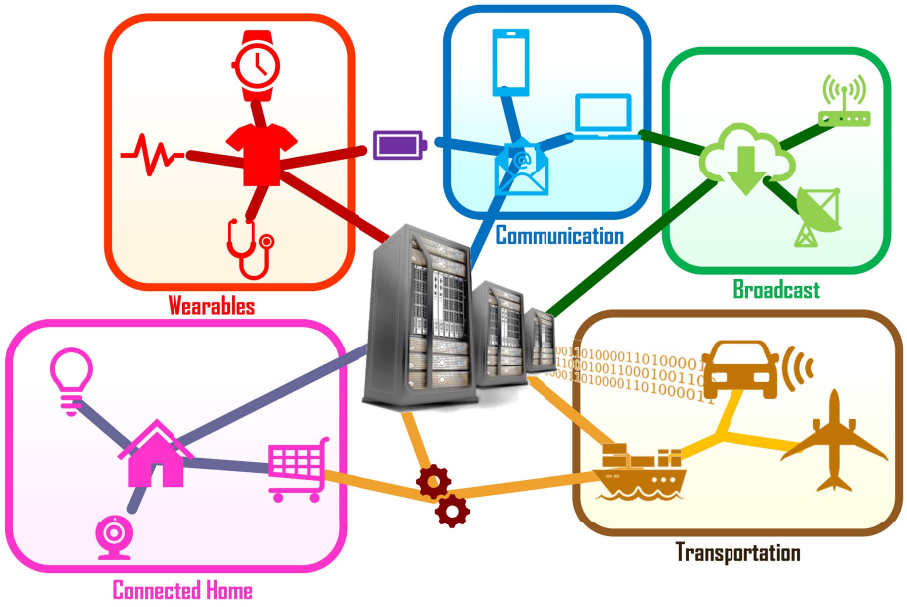

Fig. 1. Applications of cloud storage/computing used in homes, mobile devices, wearables, communication systems, and healthcare fields that require high-speed connectivity.

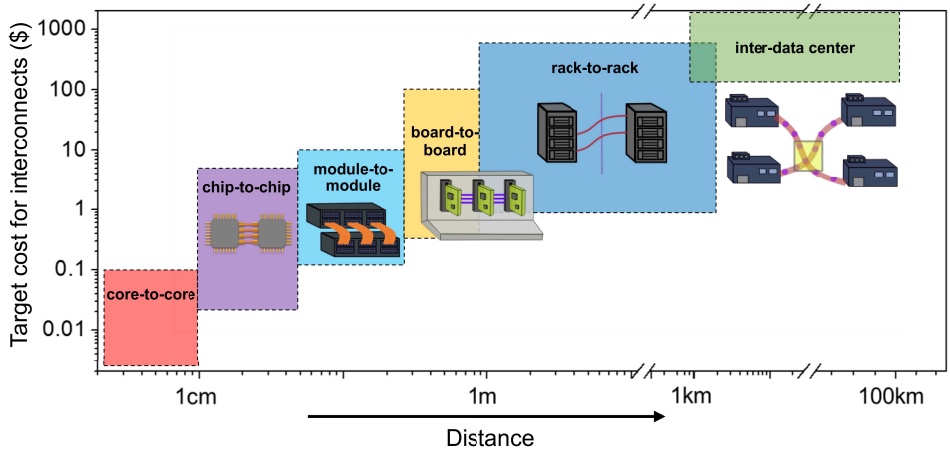

Fig. 2. Target costs for optical interconnects at various stages of data center network.

In general, the e–h pair generation in a semiconductor simply depends on the absorption length of a material. This is mainly limited by the thickness of the i-layer in a conventional p-i-n PD [Fig. 3(a)]. On the other hand, the lateral photon propagation in PDs integrated with micro-/nanoholes can result in a longer effective absorption length than the i-layer thickness [Fig. 3(b)].

Consequently, the speed of carrier collection can be increased by designing a thin absorbing layer without losing sensitivity of the PD. If the propagating light remains confined within the absorption region, an absorbing material even with a low absorption coefficient can generate e–h pairs efficiently. For example, Fig. 3(c) compares the measured responsivity of a Si PD with micro-/nanoholes reported in [4], [5] and calculated responsivity of a planar Si PD with a 2-μm i-layer and perfect antireflection coating. Si with micro-/nanoholes absorbs photons by more than one order of magnitude compared to bulk Si with the help of guided in-plane modes excited in the Si absorbing layer [4], [5].

Fig. 3(d) indicates the enhanced effective absorption coefficient ($\alpha_{\text{effective}}$) of Si with integrated holes (blue curve) based on the presented data in Fig. 3(c). As is shown in Fig. 3(c), in the range of 700–850 nm, Si with integrated holes (blue curve) exhibits an enhanced absorption coefficient and reaches a similar absorption coefficient value to GaAs (black curve) at ~850 nm. Most importantly, Si with holes can efficiently absorb light with a wavelength > 870 nm [5] which is below the room temperature bandgap of GaAs. With optimal shape, size, and device parameters of the holes, it is likely to further enhance silicon's absorption. Fig. 3(e) shows a projection of microhole-/nanohole-based Si PD's responsivity with a 10-μm i-layer (green curve) estimated by using $\alpha_{\text{effective}}$ calculated in Fig. 3(d) from empirical data. The blue curve shows the responsivity of a Si PD with a 10-μm i-layer and 2-μm deep holes simulated with the finite-difference time-domain (FDTD) method.

On the other hand, red curve represents the responsivity of similarly thick Si PD without holes. In the range

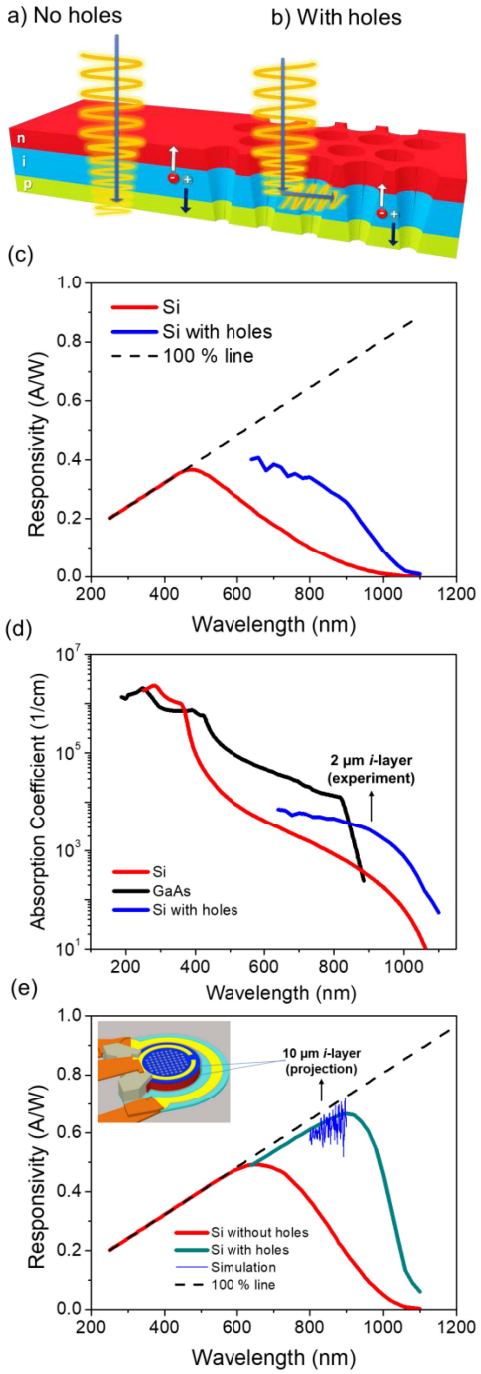

Fig. 3. (a) Schematic of a surface-illuminated planar PD with vertical carrier collection and light absorption. (b) Schematic of a surface-illuminated PD with integrated holes with vertical carrier collection and lateral light absorption. (c) Comparison of calculated responsivity of a planar Si PD with 2-μm *i*-layer with perfect antireflection coating versus measured responsivity of a Si PD with micro-/nanoholes reported in [4]. Dashed line indicates the responsivity of Si in the case of 100% absorption of all wavelengths. (d) Comparison of effective absorption coefficient ($\alpha_{\text{effective}}$) of micro-/nanostructured Si with absorption coefficients of bulk Si and GaAs between 600 and 1050 nm. Microhole-/nanohole-based PDs show an increase by an order of magnitude approaching the level of α_{GaAs}. (e) Responsivity of microhole-/nanohole-based PD with 10-μm *i*-layer estimated by using $\alpha_{\text{effective}}$ (green curve) calculated in (d) from empirical data, simulated with FDTD method (blue curve), and similarly thick Si PD without holes (red curve).

of 800–900 nm, the responsivity of PDs with holes potentially reach to the highest achievable values (considering 5% reflection from the surface), whereas the responsivity of Si without holes stays $\leq$0.3 A/W despite the thick absorption layer. Such predictions suggest that a paradigm shift in high-efficiency and high-speed Si PDs for communication can be realized by the means of low-dimensional photon absorption enhancement structures.

In this part of the review, advantages and challenges of high-speed PDs integrated with photon-trapping structures will be discussed. Most importantly, a paradigm shift in high-performance PD design for various applications such as extended-reach links, single-photon detection, light detection and ranging (LIDAR), and high-performance computing will be presented.

A. Advantages of Photon Manipulating Structures Integrated PDs

1) Cost Reduction via CMOS Integration: Si continues to remain attractive because of its low-cost and very-well established fabrication processes. For this reason, Si-based components such as modulators, couplers, waveguides, and detectors have been developed for Si photonics integrated circuits [6]. However, the indirect bandgap of Si contributes to a considerably lower absorption coefficient in Si close to its bandgap wavelengths, making it undesirable as a material of choice for high-speed PDs for short optical links. GaAs and InGaAs/InP, with their direct bandgap and higher absorption coefficient in the longer wavelengths (>800 nm), dominate market for ultrafast receivers used in short links. However, non-CMOS processing of GaAs and InGaAs/InP requires hybrid integration of PDs to the electronics used in driving and data processing circuits, contributing to higher transceiver cost. Recent demonstration of monolithic integration of nanoscale III–V devices [7], [8] by template-assisted selective epitaxy [9] can offer solutions to high-speed PD integration to VLSI-CMOS circuits but the process development and optimization of crucial parameters such as growth temperatures are highly likely to require significant investments in capital, time, and processing. On the other hand, ultrafast and highly efficient Si PDs with micro-/nanoholes [4], [5] fabricated by CMOS-compatible processes can pave the way to the integration of optical and electrical components of an optical receiver on the same chip and offer great potential to reduce the cost by 30% or more compared to what current III–V material-based technologies can offer.

2) Capacitance Reduction by Hole Arrays: Another limitation to the speed of a p-i-n PD is the junction capacitance. The 3-dB BW frequency in a typical p-i-n PD is given by [10]

$$f_{3\ \text{dB}} = \frac{1}{\sqrt{(2\pi RC)^2 + (t_{\text{tr}}/0.44)^2}}$$

where t_{tr} is transit time, R is resistance typically designed to be 50-Ω load, and C is the capacitance which is determined mostly by junction capacitance. In an ideal p-i-n diode, junction capacitance is defined as $C = \varepsilon A/d$, where A is the junction area, mostly determined by the mesa area and d is the depletion layer width which is composed of i-layer.

Integrated holes not only provide light-trapping and high optical absorption but also contribute to the reduction of the

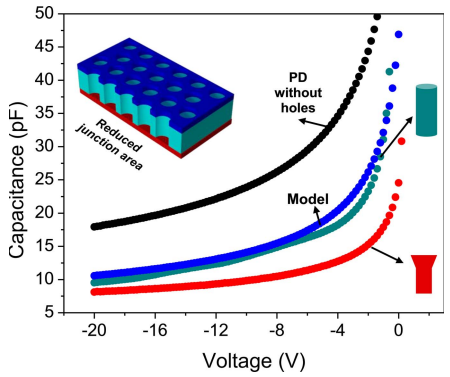

Fig. 4. Comparison of capacitance–voltage characteristics of a Si PD with no holes (black curve) cylindrical (green curve) and funnel-shaped holes (red curve). Blue curve shows a model considering the ratio of holes to the total junction area. Air holes reduce the junction area and result in considerable capacitance reduction.

junction capacitance by decreasing the junction area in an axial p-i-n diode. The inset in Fig. 4 illustrates the schematics of hole embedded axial p-i-n diode structure. Fig. 4 shows the capacitance–voltage measured from large PDs (500 μm in diameter) with and without air holes. The blue curve represents calculated C by considering reduced area caused by cylindrical air holes in the devices. It agrees well with the measured C of PDs with cylindrical holes. The capacitance reduction is enhanced by funnel-shaped holes, in accordance with larger reduction of top contact during funneling process.

B. New Technologies

1) Ultrafast, Low-Cost Optical Interconnects: Table I compares examples of high-speed PDs demonstrated in the literature for datacom applications. Generally, the data rates offered by Si p-i-n PDs are not higher than 3.5 and >10 Gb/s data rates were achieved only with an additional or integrated transimpedance amplifier and equalizer [18]. This is mainly due to the tradeoff between responsivity and bandwidth. To increase the responsivity and maintain high speed at the same time, researchers proposed and demonstrated Si PDs with various device designs. For example, a resonant cavity was introduced to Si PDs [13], [14] to multiply the optical path in the thin Si layer, which is necessary for high speed. Metal–semiconductor–metal PDs have been shown to achieve higher speed up to a few Gb/s [15], [31], but the typical QE value is around 10% and the responsivity is in the range of a few to tens of mA/W [31]. Therefore, conventional methods use PDs made of GaAs/AlGaAs material system on GaAs substrate for datacom applications between 840 and 860 nm. These PDs are designed with III–V direct bandgap material and offer high QEs [32]. However, they are not CMOS compatible and require hybrid integration or wafer bonding to be integrated into silicon electronic chips [33]. Another type of high-efficiency Si PDs that support high bandwidth are Si avalanche PDs (APDs) [19]–[24]. However, APDs usually work at a high voltage close to breakdown. Short-reach optical links require PDs powered with a dc bias around 3 V or less. The power consumption of APDs compared to their p-i-n counterparts make them unfavorable for short-reach optical links. In addition, Si APDs have a higher level of noise than that of p-i-n PDs. For long-reach communication that utilize longer operating wavelengths (1300/1550 nm) and require higher data rates, Ge-on-Si can be material of choice for low-cost and CMOS-compatible processing. Table I includes a few examples of Ge-on-Si PDs and APDs reported in the literature. However, a similar tradeoff exists for Ge-on-Si surface-illuminated PDs/APDs [27] as well. Micro-/nanostructuring of Ge can offer both high bandwidth (>50 Gb/s) and high efficiency in Ge-on-Si PDs/APDs for long-reach applications. Section V will provide a perspective on extended-reach applications such as fiber to the home and passive optical network (PON/EPON) that highly sensitive and ultrafast Ge-on-Si PDs/APDs with micro-/nanostructures can be potentially utilized.

II. Integrating Nanostructures and Challenges With Device Design

A. Electrical Contacts With Pillars/Wires

Electrical contact formation on individual nanowires and arrays of pillars poses multiple challenges that need to be addressed for integration of nanowire-/pillar-based devices to other functional circuits. Fig. 5 represents a few examples of contact formation techniques for nanowire arrays. In Fig. 5(a), the contacts on individual nanowires are aligned laterally on a substrate [34]. The contact pads are patterned and fabricated sequentially to make nanowire devices. The scalability and cost efficiency of such a technique is largely questionable. Although a laterally grown nanowire bridged in between prepatterned and highly doped semiconductor contacts [Fig. 5(b)] can yield high-quality contacts [35], light coupling to individual nanowire is extremely inefficient in the case of surface illumination. For this reason, a large area of nanowire arrays would be a more appropriate design for surface-illuminated PDs. However, the contact formation of nanowire arrays requires a technique that connects each individual nanowire from tip to tip. Fig. 5(c) shows another technique to form contacts on nanowire arrays [36]. After a benzocyclobutene layer is spin coated in between nanowire arrays, it is etched to expose the tips of the nanowires during metal or transparent oxide deposition. This technique requires additional steps for the insulation layer in between the nanowires. If the insulation layer cannot be removed, then, it can interfere with the light-trapping properties of nanowire arrays. Fig. 5(d) shows a capping method which is a combination of glancing angle and small angle deposition techniques [37]. In this method, metal or conductive oxide can be deposited on top of the nanowire array with physical vapor deposition such as evaporation or sputtering. The tip-to-tip deposition can be maintained by controlling the direction of the atomic flux, namely, decreasing the angle between the substrate normal and the flux direction gradually starting from a glancing angle such as 85°. A high angle helps the accumulation of the metal atoms at the tips of the nanowires and gradual change allows a lateral connection and forms a film-like layer at the top of the nanowire arrays.

TABLE I
PERFORMANCE COMPARISON OF HIGH-SPEED SILICON PHOTODIODES FOR OPTICAL COMMUNICATIONS

Material	Device type	Responsivity (A/W) or EQE	Wavelength (nm)	Bandwidth (GHz) or data rate (Gb/s)	CMOS compatibility and other challenges
Si [11]	p^+-p-n avalanche	0.74 A/W (at 823 nm)	850	1.6 GHz, 3.5 Gb/s	0.18 μm CMOS technology
Si [12]	p^+-n-p	N.A.	850	3 Gb/s with an analog equalizer	0.18 μm CMOS technology
Si [13]	Resonant cavity *pin*	40 % EQE	860	10 Gb/s	Complex cavity mirror fabrication
Si [14]	Resonant cavity *pin*	40 % EQE	822	10 GHz, >10 Gb/s	Complex cavity mirror fabrication
Si [15]	MSM	N.A.	850	2.5 GHz	CMOS compatible
Si [16]	lateral *pin*	47% internal QE	840	NA.	CMOS compatible
Si [17]	lateral *pin*	0.32 A/W (from 4 PDs)	850	10 Gb/s with TIA	0.13 μm CMOS technology
Si [18]	vertical *pin*	0.26 A/W	850	11 Gb/s	Modified 0.5 μm BiCMOS technology
Si [4]	vertical *pin*	52% EQE at 850 nm	broadband absorption between 800-900 nm	>20 Gb/s	CMOS compatible
Si [19]	APD	0.07 A/W	850	5 GHz, 12.5 Gb/s with equalizer circuit	0.25 μm Si/Ge BiCMOS technology
Si [20]	APD	10% EQE	850	8 Gb/s	0.13 μm CMOS technology
Si [21]	APD (double PD)	0.84 A/W	850	0.7 GHz	40 nm CMOS technology
Si [22]	Spatially-modulated APD	0.18 A/W	850	8 GHz, 12.5 Gb/s with TIA, equalizer and limiting amplifier	0.13 μm CMOS technology
Si [23]	APD	4.67 A/W	850	10 Gb/s	0.13 μm CMOS technology
Si [24]	APD	2.94 A/W	850	3.2 GHz > 1THz GB product	65 nm CMOS technology
Nano-structured Si [25]	SPAD	32% PDE*	850	25 ps (FWHM)	CMOS compatible
Ge on Si [26]	*pin*	0.9 A/W (at 1310 nm)	800-1360	10 Gb/s	Limited CMOS compatibility
Ge on Si [27]	vertical *pin*	0.21 A/W	1500	40 Gb/s	CMOS compatible
Ge on Si [28]	APD	N.A.	830-1000	25 Gb/s	Limited CMOS compatibility Hard to couple fiber due to small aperture (20 μm)
Ge on Si [29]	APD	0.4 A/W	1300	>30 GHz	CMOS compatible expensive packaging for waveguide APD
Ge on Si [30]	APD	5.88 A/W (at 1310 nm)	1300	>30GHz, and 340GHz GB product	CMOS compatible

*Photon detection efficiency.

B. Contacting a PD With Integrated Holes

Alternatively, subtractive micro-/nanostructure arrays such as arrays of holes, cones, and funnels are the most advantageous structures for contact fabrication. A metal ring around active area that has arrays of holes can be patterned and fabricated with conventional CMOS-compatible methods already used for planar PDs, as shown in Fig. 5(e).

C. Surface Traps, Persistent Photocurrent, and Surface Passivation

One of the noise components in the PDs is the dark current. In an ultrafast PD, the dark current is expected to be under the nanoampere range. However, high surface area of pillars/holes, which are ideal in photon-trapping PDs, also introduce a high density of surface states which remain electronically active if not passivated with high-temperature processes or surface treatments via chemicals. The charges at the surface states can contribute to the current by thermionic emission and increase the current even under no illumination [38]. In addition, these surface states act as recombination centers for photo-generated carriers which can be trapped by unpaired dangling bonds on the surface. Surface states decrease the efficiency of nanowire solar cells by several percentages [39]–[41]. As illustrated in Fig. 6(a), electron–hole pairs are generated in the core part of the nanowire due to the light illumination. The single Fermi level E_F in the dark corresponding to the n-type nanowire splits into a quasi-Fermi level for electrons $E_{\mathrm{Fn}} - E_F$ (no practical change in the majority carrier density) and that for holes $E_{\mathrm{Fp}} < E_F$ (appreciable increase in the minority carrier density) in the core. Near the nanowire surface, there are surface states and the dark Fermi level is pinned, resulting in band bending at the surface. The surface states serve as strong recombination centers and the generated electrons and holes recombine there. This causes the split quasi-Fermi levels E_{Fn} and E_{Fp} to be united at the surface [42].

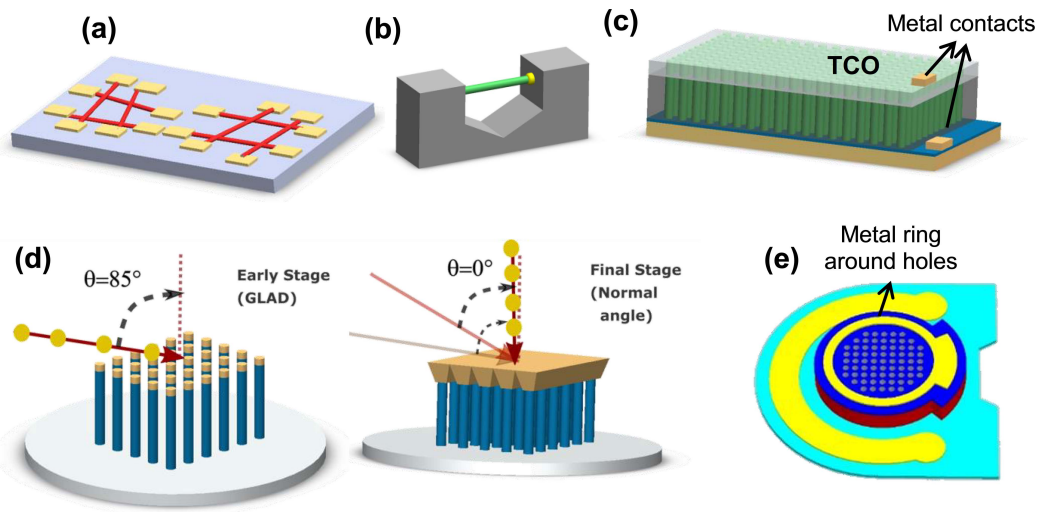

Fig. 5. (a) Selective contact formation on individual nanowires. (b) Lateral growth of nanowires on highly doped substrates. (c) Embedded insulation layer technique in between nanowires. (d) Capping technique which is a combination of glancing angle and small angle deposition techniques. (e) Lithographically patterned metal ring around arrays of nanoholes.

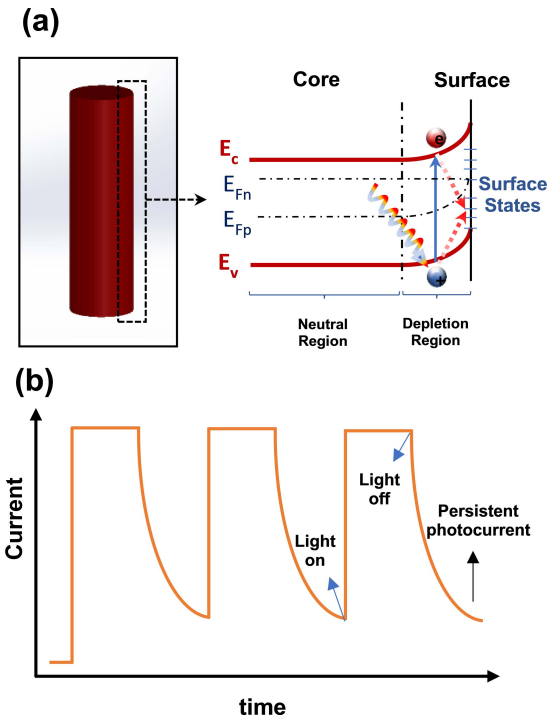

Fig. 6. (a) Schematic of a nanowire with corresponding energy band diagram near nanowire surface under illumination is illustrated. High density of surface states causes a depletion region due to Fermi level pinning at the surface of the nanowire. This region provides efficient charge separation; photo-exited electrons are forced to flow to the nanowire (n-type) core and holes are trapped at the surface. This helps photo-exited carriers live longer and makes surface recombination almost impossible. (b) Illustration of typical photo response gained from nanowire photoconductor. Although, surface states result in high gain, it comes at a cost of slow relaxation of carriers to the ground state, causing persistent photocurrent.

In a solar cell, photo-generated minority carriers must be brought to the electrodes via the diffusion process. Accordingly, the extra surface recombination prevents the minority carriers from reaching to the junction and generating electricity. That is why, in earlier studies, nanowire-based solar cells generally exhibited extremely low efficiencies compared to thin film counterparts LATER, the efficiency of nanowire-based solar cells increased with the introduction of effective passivation layers [42]–[44]. On the other hand, the drift process in p-i-n photodiodes due to reverse bias can offer an advantage for effectively collecting the carriers before they are trapped at the surface, but, the existence of the surface states can still pose a challenge because a strong electric field is required for effective carrier collection. On the other hand, the applied field to a practical p-i-n PD needs to be limited to ∼3-V reverse bias. For this reason, an effective surface passivation is necessary to ensure high efficiency in a practical p-i-n PD.

The scenario is slightly different in the case of nanowire-based photoconductors. The nanowire surface is generally depleted in the dark, and negligible current flows near the surface, resulting in a low dark current. Under illumination, electron–hole pairs are generated and a significant amount of current flows even near the surface, as shown in Fig. 6(a). Thus, photocurrent to dark current ratio is high in the nanowire-based photoconductor, resulting in high gain. Many studies have reported nanowire photoconductors with extremely high gain and these studies were extensively reviewed in [45]. In most nanomaterials, once optical illumination is terminated, it takes photo-generated carriers a long time to recombine and thus, increases the recovery time which results in persistent photocurrent [Fig. 6(b)] [46]–[49]. Persistent photocurrent can cause signal distortion due to the long fall times of the carriers. Therefore, surface passivation is needed to prevent the persistent current and suppress the dark current, which contributes to the noise.

Surface passivation of surface-textured devices could be attained by chemical or field effect passivation techniques [38], [50], [51]. Chemical surface passivation such as termination of dangling bonds by hydrogen have been applied for mate-

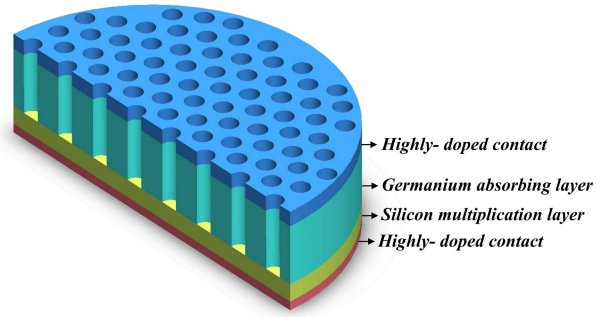

Fig. 7. Schematic of APD with photon-trapping structures.

rials that have s–p orbitals crossing such as Si, Ge, and GaAs [38], [51]. Thermal oxidation is another widely used technique for surface passivation purposes. Field-effect-based surface passivation can be acquired by depositing a fixed charged thin layer which drives minority carriers away from surface states due to the built-in electric field [38], [50].

III. Future Opportunities

A. Photon-Trapping Avalanche Photodetectors (APDs) for Extended-Reach Links

APDs can have high gain due to charge multiplication, whereas p-i-n PDs inherently have a maximum of unity gain. Therefore, APDs can offer more advantages than p-i-n PDs for extended-reach optical links where 1550 nm is the wavelength of operation. For this reason, Si solely is not a material of choice in APDs for long-reach applications. Germanium (Ge), with a narrower bandgap is currently a material of interest in APDs as the absorbing layer for 1300 nm and tensile-strained Ge is capable of absorbing around 1500 nm [52]. By contrast, Si has been proven to be the best material as a charge multiplication layer for its favorable ionization coefficient ratio and very low-temperature dependence of the avalanche breakdown [53]. Therefore, Ge-on-Si is a promising material system in APDs for extended-reach applications. Fig. 7 illustrates a possible design of Ge-on-Si APDs where the micro-/nanoholes can be integrated into the Ge absorbing layer to provide a broadband and high photon absorption.

There are Ge-on-Si APDs available for 25 Gb/s operation at 1310 nm in the market [28]. In [29], a Ge-on-Si APD is reported for 1300-nm operation with a bandwidth above 30 GHz. Integrating holes into the absorption layer of Ge-on-Si APDs can offer efficient coupling of the incident light with longer wavelengths. APDs with photon-trapping micro-/nanostructures can extend the range of APD operation to the *C*-band (1550 nm) from existing operating bands (1300 nm) at 25 Gb/s data transmission rate. On the other hand, the large lattice mismatch of 4.2% between Ge and Si [54] can cause large dislocation densities which would reduce the carrier mobility, increase the dark current, and prohibit the economic yields of device in VLSI or ultralarge-scale integration production [55]. Although the stressed Ge films on Si show higher absorption at longer wavelengths (∼1500 nm), the reproducibility of stressed Ge films on Si is still questionable. Alternatively, micro-/nano structuring of Ge-on-Si can be a better solution to produce high-efficiency PDs/APDs for extended-reach applications with high data transmission rates.

B. Single-Photon Avalanche Detection (SPAD) for Quantum Communication and LIDAR

The information age brings its challenges, especially in secure data transmission. Quantum communication is predicted to be the most secure technology for data transmission. Since tapping to the transmission line can destroy the quantum states of entangled photons, immediate detection of a tapped line will be possible in a quantum communication system (QCS) [56]. Single-photon detectors are the main component in the receiver of a QCS. Emerging technologies such as superconductor single-photon detectors [57], [58] are on the rise. However, technical challenges such as cooling requirements do not allow them to be practical devices yet [59]. Currently available photon counting systems have single-photon avalanche diodes (SPADs) operating at above breakdown voltage, known as Geiger mode APDs [60]. Such SPADs become standard in photon counting which is a major tool in quantum communication and LIDAR applications.

As presented in [61], SPADs fabricated with CMOS technologies have thin-planar layers that can provide high resolution in photon timing which is dominated by transit time of the carriers from absorption region to the multiplication region. However, high photon timing resolution with thin layers comes at the expense of low photon detection efficiency (PDE), especially for longer wavelengths (for example, 15% at 820 nm [60]). Relatively low breakdown voltage is necessary if the SPAD has a thin depletion layer, which causes relatively low PDE. Ghioni *et al.* [62], [63] demonstrated resonant-cavity-enhanced SPADs with a 34% PDE at 850 nm; however, as mentioned earlier, resonant cavity-based PD designs suffer from narrow optical bandwidth. For a broadband and high-efficiency SPADs sandwiched between SiN nanocone arrays are proposed recently [64]. In addition, Ge-on-Si SPADs have been demonstrated for single-photon operations at 1310 and 1550 nm with a 4% and 0.15% single-PDE [65] SPADs are also recently proposed for visible light communication systems [66], [67] due to their high sensitivity to weak illumination transmitted from long distances. Integrating photon-trapping structures such as micro-/nanostructured holes into SPADs can improve PDE over a similar SPAD without micro-/nanoholes [25].

C. CMOS Integration

Currently, high-speed III–V and Ge PDs have been integrated with the CMOS chips through flip-chip technology, wafer bonding or wire bonding techniques [68]. However, these technologies are not CMOS compatible and require complex fabrication processes. The yield of these processes is low and such hybrid integration can result in high noise. On the other hand, monolithic integration can give the designer control of capacitance and reduce the noise. The cost of these monolithically integrated chips can be dramatically low.

IV. Conclusion

The opportunity of high-speed and high-efficiency PDs with CMOS-compatible material systems such as Si, SiGe, and Ge-on-Si can pave the way to low-cost optical interconnects that are easily adaptable to wide range of applications in modern data centers. However, device design and fabrication related challenges need to be addressed to tap into the true potential of light-trapping features. The grand challenges of nanostructured PDs include the following:

1) lack of practical solutions for manufacturing electrical contacts;
2) high-leakage current and surface recombination caused by high density of surface states due to high surface to volume ratio structures;
3) high resistance caused by minimized material;
4) insufficient light coupling in the case of single nanowire PDs;
5) incompatible size of plasmonic structures to CMOS processing.

The nature of negative structures such as holes, inverted pyramids, or cones can keep the surface material contiguous and offer a solution to the first challenge by designing contacts that can be fabricated with CMOS-compatible conventional processes. On the other hand, the challenges listed in 2) and 3) are valid for negative structures as well. Therefore, CMOS-compatible surface passivation techniques need to be developed to realize practical Si PDs with micro-/nanostructures. Inherently, having less material compared to bulk counterparts, micro-/nanostructures cause an increase in resistance, which can limit the speed of a photodiode. However, this drawback can be suppressed with smart designs of micro-/nanostructures to reduce the capacitance at the same time. Reduction in capacitance can compensate for the increase in resistance and eliminate *RC* time limited response. The structures in subwavelength size ($<$900 nm) are challenging to pattern with conventional optical lithography. However, DUV lithography can address this challenge in the VLSI-CMOS process lines. Even though there are challenges that need to be addressed to benefit from the full potential of Si-based PDs with micro-/nanostructures, the advantages of monolithic integration and reduced cost of the transceivers that utilized such PDs, promise real solutions to meet the high demand of connectivity in modern data centers that are expected to connect numerous computer systems serving artificial intelligence, the IoTs, autonomous vehicles, and social infrastructures.

Given the complexity of the Si PD and CMOS circuit integration and the diversity in designing PDs, this review is by no means exhaustive. This review is intended to provide a glimpse of the technical and integration challenges in designing PDs for ultrafast communication links and serves as a document on advanced research activities in ultrafast Si detectors for communication including single-photon communication and quantum communication. We believe that the Si-based ultrahigh-speed photodiodes will contribute to high-performance VLSI receivers and will represent an important modality within the short as well as long-range communication links.

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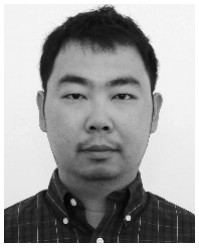

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