High-Speed High-Efficiency Photon-Trapping Broadband Silicon PIN Photodiodes for Short-Reach Optical Interconnects in Data Centers

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***Abstract*—Monolithic integration of high-speed, high-efficiency photodiodes with receiver electronics on a single silicon chip is a key to reduce cost and improve the performance of data centers' short reach optical interconnects. We report a CMOS-compatible surface illuminated silicon PIN photodiode with integrated micro- and nano-scale holes that trap photons for longer interaction with semiconductors resulting in higher absorption efficiencies. The fabricated photodiode demonstrates more than 55% external quantum efficiency (EQE) at 850 nm, and a measured Full-Width at Half Maximum (FWHM) impulse response of 29 ps, 31 ps, and 34 ps at 15 V, 10 V, and 3 V reverse biases, respectively. Simulation results indicate the possibility of operation up to 12.5 Gb/s (NRZ) with no equalization.**

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I. Introduction

A 24 PERCENT compound annual growth rate (CAGR) is estimated for global internet protocol (IP) traffic from 2016 to 2021 with a data volume of 3.3 ZB per year [1]. The massive traffic growth is due to the next generation of wireless networks, the emergence of new cloud-computing systems, Internet of Things (IoT), and worldwide online multimedia streaming services. To handle the explosive internet traffic load, data centers are expanding rapidly with new architectures handling higher traffic volumes relative to the Internet. The amount of annual global data centers traffic in 2018 is estimated to be 11.6 ZB and by 2021 will reach 20.6 ZB [2], [3], with 70% of this traffic residing within the data center [2]–[5]. Current data centers widely use low-cost and energy efficient optical interconnects and that is expected to continue in the future. Nowadays, low cost, broadband, and energy efficient optical interconnects based on vertical cavity surface emitting lasers (VCSELs), multimode fiber (MMF) and III-V material-based PIN photodiodes (PDs) are commonly deployed technologies in the high-speed optical short-reach links (<300 m) in data centers. Transmitters (T_x) using extremely low power (1 pJ/bit) CMOS-compatible VCSEL drivers can work properly in 25 Gb/s optical links. SiGe drivers can reach even higher speed up to 80 Gb/s over 300 m link lengths [6]–[9]. However, on the receiver side (R_x), it is very challenging to design both photodiode and transimpedance amplifier (TIA) with high bandwidth and high efficiency to adopt such data rates.

In general, column III-V PDs (such as GaAs or $In_x Ga_{1-x} As$) and CMOS or SiGe amplifiers are designed and fabricated separately. Using an optimized wire bonding process, the devices are packaged together after fabrication. This method is challenging

for large-scale production, and it is complicated and expensive to be used for connecting an array of photodiodes to an array of amplifiers. Moreover, undesirable packaging parasitic (such as inductance and capacitance) degrade the high-speed device performance and cause electrical crosstalk between channels.

Silicon (Si) due to high reliability, low-cost mature fabrication process, and volume manufacturability is the best candidate to produce low-cost high-speed optical PDs. Using the CMOS fabrication standards, both Si PD, silicon-based transimpedance amplifiers (TIA) and clock data recovery circuits (CDR) can be monolithically integrated on the same chip. Optical transceiver cost per Gb/s is an essential issue in data centers. Currently, the average cost per Gb/s is in order of tens of dollars, which needs to be decreased to few dollars [10].

Two types of Silicon PIN photodiodes have been demonstrated. Lateral PIN PDs have been developed via a simple CMOS-compatible fabrication process. Similar to the source and drain fabrication steps of CMOS transistors, the interdigitated p and n-regions can be formed on top of the i-layer. A 75 μm diameter Si PD (discrete lateral trench detector (LTD)) using Si deep-trench DRAM technology integrated with SiGe TIA reached 2.5 Gb/s high-speed performance with 68% EQE at 845 nm (3.3 V bias) [11]. A PIN lateral photodiode on a silicon-on-insulator (SOI) substrate with 2 μm thick device layer integrated with 130 nm high-performance MOSFET (HIPER-MOS) reported $\sim$10% EQE at 847 nm and up to 3.125 Gb/s under -3 V bias [12].

In order to design a surface-illuminated Si PIN PD (vertical PIN structure), trade-off between high-speed and EQE needs to be taken into consideration. A relatively thick absorbing layer is required to achieve reasonable optical efficiency. However, carrier transient time increases with the length of absorbing medium which limits the device bandwidth. A 50 μm diameter PIN PD with 10 μm length absorbing region achieved 3 dB bandwidth of 2.2 GHz at 17 V bias. Monolithic integration of the PD with an analog equalizer enabled up to 11 Gb/s high-speed performance [13].

Vertical PIN Si-photodiodes fabricated on silicon on insulator (SOI) are also proposed and studied by the optical short-reach community. Surface illuminated resonant-cavity-enhanced (RCE) PIN PDs have been proposed for high bandwidth applications [14] using a thin absorbing layer inside a Fabry-Perot resonant cavity with a two-period distributed Bragg reflector (DBR). The reported RCE device exhibited a 40% EQE at 860 nm and an impulse response of 29 ps FWHM for 30 μm diameter at 9 V bias. However, RCE devices are wavelength specific, and CMOS-compatible fabrication issues have remained unsolved.

Recently, an innovative approach was applied to enhance the efficiency of CMOS-compatible surface illuminated Si PDs using NIP structure on SOI wafers for high speed operation with photon-trapping structure [15]–[18]. A detailed performance comparison of Datacom Si photodiodes is presented in Ref. 18.

In this article, a vertical CMOS-compatible surface-illuminated PIN Si PD on SOI wafers with integrated photon-trapping structure is studied [19]. The surface light-trapping structure combined with silicon oxide has offered a solution to both the challenges of low speed and low EQE. Integration of optimized micro/nanoholes on the surface of a 2 μm thick absorbing region with a 30 μm diameter, has resulted in more than 50% EQE and deconvolved FWHM response of $\sim$19 ps, $\sim$21 ps, and $\sim$23 ps for 15 V, 10 V, and 3 V at 850 nm, respectively (relative to a measured response of 29 ps, 31 ps and 34 ps, respectively). A PD model including a carrier transport mechanism, an equivalent device circuit model, and a tail extrapolation block is developed based on the measured impulse response. The effect of measurement setup and the pulsed laser is considered to reach a realistic PD model. The measured impulse response data at different biases are in close agreement with the results of the model. Simulated eye-diagrams at 8 Gb/s, 10 Gb/s and 12.5 Gb/s without equalization using the PD model are presented and discussed. Future devices with minimum tail combined with 2-tap Feed-Forward pre/de-emphasis equalizers are modeled. The results show that highly efficient future Si-based PDs have the potential to be operational up to 50 Gb/s.

II. Device Design and Fabrication

The cross-section schematic of Si-PIN PD is depicted in Fig. 1(a). The photodiode was fabricated on a Silicon-on-insulator (SOI) substrate that includes a 0.2 μm low-doped p-Si device layer, 3 μm buried SiO_2 box layer, and 625 μm thick Si handle wafer (not shown in the Fig. 1). The thin-film PIN structure with the 2 μm active region (i-layer) and heavily doped n-Si bottom contact as well as p-Si top contact with 0.3 μm thickness is designed to minimize the transport time of photo-generated electron and holes in absorbing medium.

Micro/nano-scale hole array -with square and hexagonal patterns- are integrated on the surface of the PD's absorbing region to enhance the absorption of photons with energy (1.45 eV at $\lambda = 850$ nm) close to silicon band gap (1.12 eV). The hole arrays were etched (2.3 μm deep) up to the n-Si layer with both cylindrical and funnel shape profile in different devices.

A set of simulations were performed to obtain an optimum design for surface nanostructures that can offer the maximum optical absorption in the 850 nm window [15], [16]. After evaluating the simulation results, 2D hexagonal and square periodic nanohole patterns with different diameter/period (*d/p*) of 1300/2000 nm and 700/1000 nm were chosen to fabricate Si PDs. Bottom contact, an active region, and top contact were epitaxially grown using Chemical Vapor Deposition (CVD) method. To boost the speed of the device, p- and n-layer doped to the level of $5 \times 10^{20}\text{cm}^{-3}$ (boron-doped) and 10^{19}cm^{-3} (As-doped) were grown to minimize the recombination time of diffused minority carriers in contact layers. The active layer (i-layer) was slightly unintentionally doped to n-type characteristics ($\leq 5 \times 10^{16}\text{cm}^{-3}$) during growth process. Doping profile of the fabricated PIN devices is shown in Fig. 1(b).

The doping profile shows that there are transition regions at both n^+ and p^+ boundaries with i-layer. This contributed to a reduced effective absorbing medium of less than 2 μm. Deep reaction ion etching (DRIE) and RIE techniques were used to form cylindrical or funnel-shaped micro/nano holes, respectively. The diameters and sidewall angles of holes vary

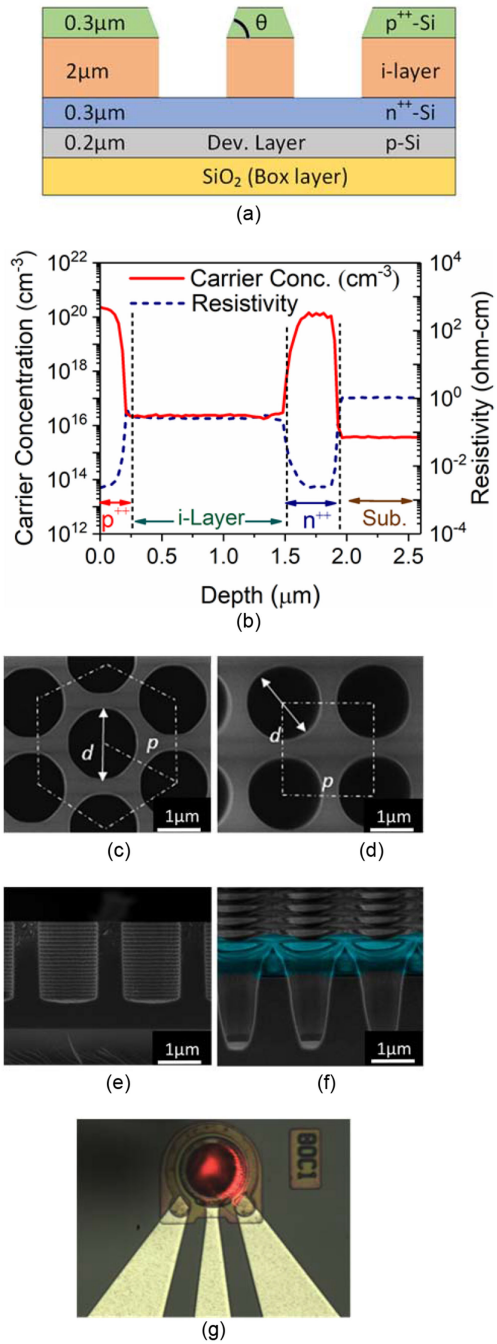

Fig. 1. (a) Schematic cross-section of designed Si PIN PD integrated with light-trapping holes on an SOI wafer. (b) Doping profile of the fabricated device, transient doping regions at the p^{++}-i and n^{++}-i interfaces are depicted. SEM micrograph of micro/nano hole surface arrays. (c) Hexagonal and, (d) square pattern (top view). (e) Cylindrical and, (f) funnel-shaped micro/nano hole (cross-section), and (g) a 30 μm PD with CPW (under illumination) that used for DC and RF characterization.

as indicated by scanning electron microscopy (SEM) images Fig. 1(c)–(f). Subsequent to mesa isolation, aluminum (Al) ring contacts were deposited on n^+ and p^+ regions to facilitate photo-generated carrier collection. To conduct wafer-level high-speed measurements, Al co-planar waveguide (CPW) is designed with 50 Ω characteristic impedance. An optical image of the 30 μm diameter device that was used for DC and RF characterizations is depicted in Fig. 1(g).

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III. Optical Characterization

Absorption enhancement in thin-film photodetectors with normal to surface illumination requires light-trapping structures to confine photons in the active region. The periodic nanohole arrays in our devices have been found to excite lateral propagating modes facilitating longer photon-material interactions [15]. Measurement shows that absorption is enhanced for arrays with $d/p = 700/1000$ nm holes (larger number of holes per area) combined with the silicon dioxide layer that helps to confine light into the absorption layer. To compare the performance of the devices with and without micro/nanoholes, we fabricated control devices without holes in the same processing line. The devices with micro/nanoholes have exhibited strong coupling of the vertically oriented incident plane waves into a multitude of lateral modes in the active region [15]. Optical absorption (EQE) of both flat and patterned ($d/p = 700/1000$ nm) devices are presented in Fig. 2(a). The devices exhibited more than 55% EQE at 850 nm wavelength for the PDs with funnel-shaped holes ($\theta = 61^{\circ}$) that are arranged in hexagonal arrays and more than 37% EQE for devices with cylindrical holes. By contrast, the devices without integrated micro/nanoholes exhibited less than 9% EQE. Therefore, a significant absorption enhancement of four times for cylindrical holes and six times for funnel-shaped holes is achieved compared to the devices with flat surface (Fig. 2(a), blue and green colors).

To evaluate the efficiency of the light-trapping structures, the enhanced absorption coefficient (α_{eff}) is calculated via (1):

$$\alpha_{eff} = -ln\,(1 - A)\,/L \tag{1}$$

where A is the measured absorption and L is the absorbing layer thickness. Fig. 2(b) compares the effective absorption coefficient (α_{eff}) of our devices with bulk silicon (α_{Si}) and GaAs (α_{GaAs}) which is the dominant material used in high-speed high-efficient PDs due to its direct band gap. It implies that designed Si PIN PDs integrated with surface nanohole arrays have broader absorption spectrum compared to GaAs-PD, which makes the device suitable for transceivers design for new short wavelength division multiplexing (SWDM) [8]. Moreover, to reach the same

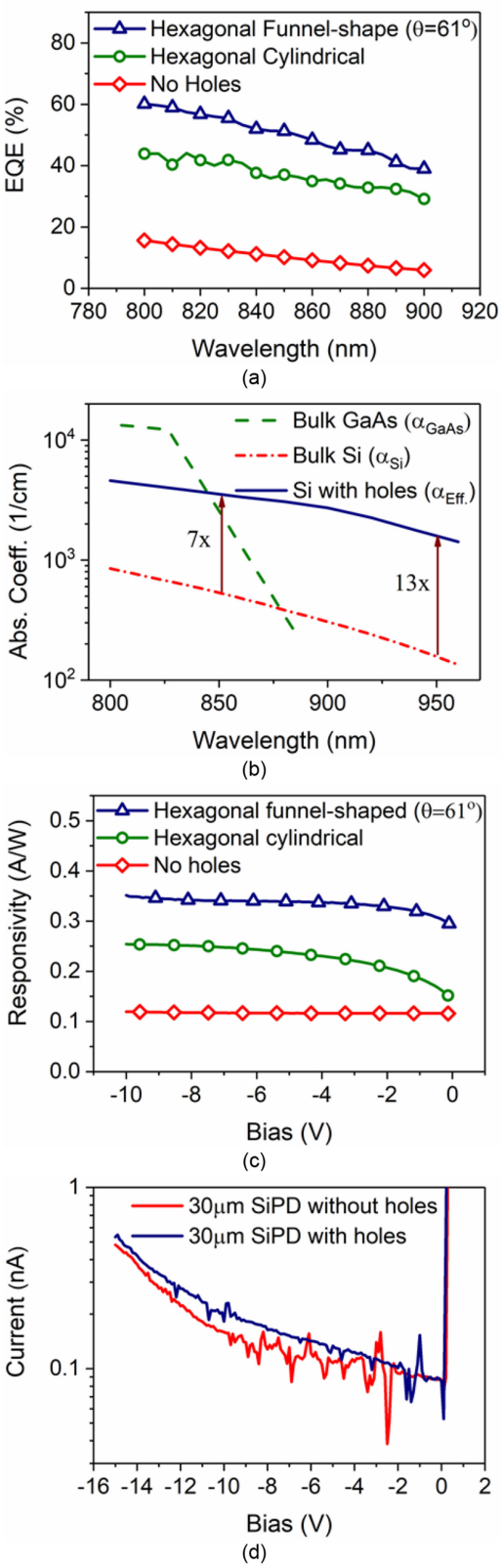

Fig. 2. (a) Optical absorption (EQE) for devices with integrated cylindrical/funnel-shape micro/nano holes and devices without surface patterning. (b) The effective absorption coefficient of Si with integrated micro/nano holes on the surfaces compared to bulk GaAs and Si, (c) Responsivity vs. bias voltages for devices with and without integrated hole Responsivity vs. bias voltages for devices with and without integrated hole array, (d) Measured dark current of 30 μm devices with both flat and nanostructured surface.

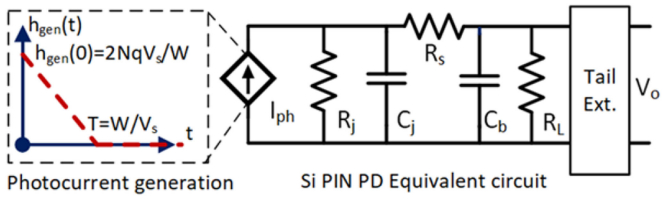

Fig. 3. PD model including the photocurrent generation mechanism block followed by PD equivalent circuit and a tail extrapolation algorithm block. The circuit parameters are extracted from the I-V and C-V measurements.

optical absorption (55%) in PDs with flat surfaces, 13 times thicker absorbing region is required.

Responsivity – the capability of Si PIN PD to convert incident illumination power into electrical current – as a function of reverse bias is shown in Fig. 3(c) for $\lambda = 850$ nm. Due to higher optical absorption in the devices with integrated micro/nanohole array, the responsivity is enhanced to 0.33 A/W (at 3 V) compared to 0.11 A/W exhibited by flat devices. We also observed that (Fig. 2(c)) the responsivity is almost voltage independent for higher reverse bias after 3 V.

The results of the DC measurement of the fabricated devices with 30 μm diameters on the same wafer with identical physical parameters are shown in Fig. 2(d). The Current-Voltage (I-V) measurement was done using a semiconductor parameter analyzer (Agilent 4156b). Both 30 μm diameter devices with and without micro/nanoholes demonstrated less than 1 nA dark current. The higher dark current of surface patterned devices is due to the surface damages occurred during the DRIE process. The series resistance of 30 μm devices with surface nanoholes was measured to be $\sim$83 Ω using I-V characteristics in forwarding bias regime.

IV. Device Model and RF Characteristics

The PD model includes a photocurrent generation mechanism block followed by the PD equivalent circuit and a tail extrapolation algorithm block is shown in Fig. 3.

To obtain accurate Si PIN PD model parameters, the effect of the on-wafer probe has been included in the equivalent circuit model. Therefore, PD equivalent circuit consists of junction capacitance (C_j), series resistance (R_s), and large shunt resistance (R_j); is connected to bonding capacitance (C_b) and 50Ω load resistance (R_L). The series resistance and combination of junction-bonding capacitors $(C_j + C_b)$ are obtained from the device I-V (forward bias) and C-V (reverse bias) measurements, respectively. Photocurrent generation in depletion region has been modeled based on the assumption of uniform electron-hole generation along the depletion region with a triangular impulse response $h_{gen}(t)$ versus time [20] $(h_{gen}(0) = 2NqV_s/W)$ where N is electron-hole count, q is electron charge, and V_s is the silicon carriers saturation velocity in depletion region (W). An extrapolation algorithm is used to include the effect of measured tail on the PD model.

Capacitance measurement (at 1 MHz) was conducted for devices with various diameters (20–80 μm) using a precise LCR meter (Agilent 4284 A). The applied electric field over device

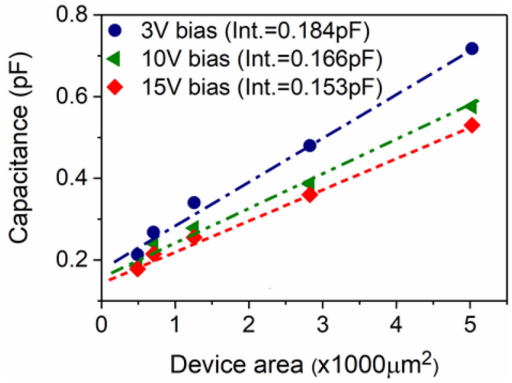

Fig. 4. Extraction of junction (C_j) capacitance, bonding (C_b) capacitance, and depletion region width (W) using a linear interpolation of devices with the different capacitance at certain voltages, 3 V, 10 V and 15 V.

TABLE I
MEASURED 30 μM DEVICE PARAMETERS VS. BIAS

Table 1. Measured 30μm device parameters vs. Bias				
Bias	R_s (Ω)	C_j (pF)	C_b (pF)	W (μm)
3V	83	0.084	0.18	0.9
10V	83	0.075	0.17	1.3
15V	83	0.06	0.15	1.4

contacts controls the thickness of the depletion region formed in the i-layer. Therefore, lower PD capacitance in higher reverse voltages is the consequence of increased depletion region.

In order to find the individual equivalent circuit capacitances (C_j and C_b) and the depletion region width (W), a linear interpolation method was employed to the capacitance of the devices with the various area (A) at a given voltage. Assuming that the surface nanostructure has an insignificant effect on the device capacitance, (2) reflects the linear interpolation of the measured capacitance-area:

$$C = C_j + C_b = (\varepsilon_{Si} A/W) + C_b \tag{2}$$

Where ε_{Si} is silicon dielectric constant. The linear interpolation slope (ε_{Si}/W) and intercept (C_b) is presented in Fig. 4 for 3 V, 10 V, and 15 V biases. The device equivalent circuit parameters and the depletion region thickness extracted from I-V and C-V measurements are presented in Table I for 30 μm devices.

Unintended dopant diffusion from n^+ and p^+ regions to the active layer during epitaxial growth caused a smaller i-layer thickness relative to the original design value of 2 μm. An optimized growth process to ensure abrupt junctions (p-i and i-n) can inhibit the dopant diffusion issue and effectively restore the active region to 2 μm in our future devices.

Wafer-level RF measurement was conducted using a microwave probe (GSG, Cascade) for devices with 30 μm diameter containing hexagonal holes arrays with d/p = 700/1000 nm. A mode-locked pulsed laser (Calmar Laser Inc.) with 850 nm center frequency, 20 MHz duty-cycle, and the sub-picosecond (200fs) pulse width was used on a probe station as a surface illuminating light source. The FWHM of the laser pulse delivered to the PD surface was increased to ~5 ps due to propagation

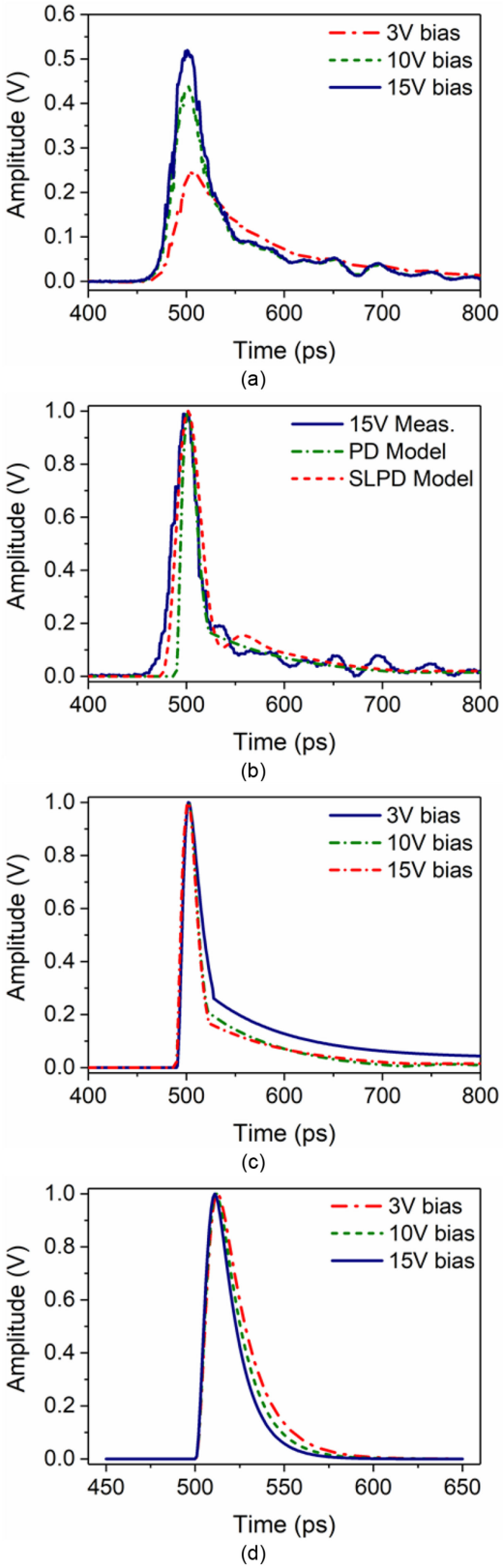

Fig. 5. (a) Measured impulse response at different voltage bias. FWHM is measured 29 ps (navy), 31 ps (green), 34 ps (red) at 15 V, 10 V, 3 V, respectively. (b) Comparison of measured (navy), PD model (green), and Scope-PD-laser (SLPD) (red) impulse response at 15 V, (c) PD model at 3 V, 10 V, and 15 V, (d) PD model for future devices shown in Fig. 3 without tail extrapolation block.

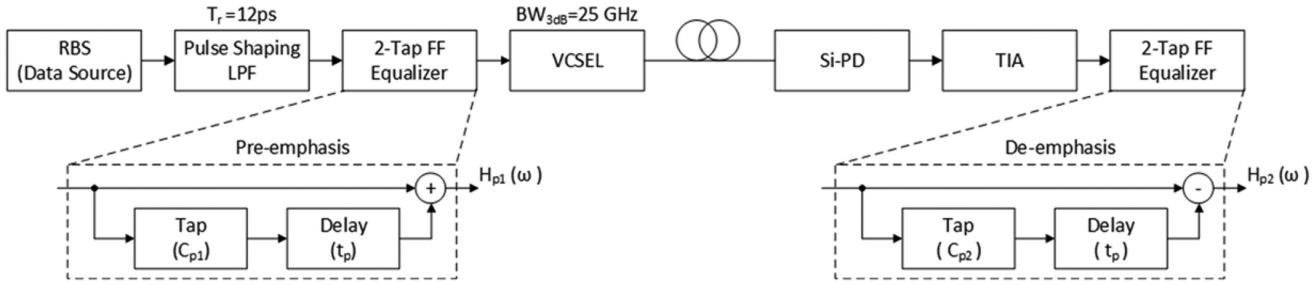

Fig. 6. Full optical link consists of a transmitter, multimode short-reach fiber, and receiver. T_x includes random bit source (RBS), pulse shaping amplifier, 2-tap pre-emphasis FFE, VCSEL. R_x includes Si PIN PD, transimpedance amplifier (*TIA*), and 2-tap de-emphasis FFE.

through few meters of fiber. The light beam was aligned close to normal to surface to reach maximum photocurrent. The device output signal recorded by a sampling scope with 3 dB bandwidth of 20 GHz (DSA8300, Tektronix).

The measured impulse response of the 30 μm device is recorded in 800 ps (0.8 ns) window with 1 ps (1 GHz) resolution (shown in Fig. 5(a)). Due to the variation of depletion region width at different biases, as discussed previously, the impulse response is also voltage dependent. The FWHM of Si PIN PD at 3 V, 10 V, and 15 V biases were measured to be 34 ps, 31 ps, and 29 ps. Based on the design considerations, the tail followed by fall time was expected to be much smaller than the observed results. However, the additional tail after the pulse fall time is due to the slow diffusion of photogenerated minority carriers at the p-i and i-n interfaces caused by unintended dopant diffusion, as was described earlier.

The effect of measured unexpected extra tail is imported to the PD model using a nonlinear fitting algorithm (Fig. 5(b), green color). Also, the effect of the measurement equipment including sampling oscilloscope (3 dB bandwidth: 20 GHz modeled as a third order Butterworth filter) and pulsed optical laser (FWHM: 5 ps) on the measurement was combined with the PD model to form the Scope-Laser-PD model (SLPD model). There is a strong agreement between the SLPD model (Fig. 5(b), red color) and measured impulse response (Fig. 5(b), navy color).

The deconvolved impulse response for the fabricated 30 μm device at 15 V, 10 V, and 3 V are shown in Fig. 5(c) with FWHM of $\sim$19 ps, $\sim$21 ps, and $\sim$23 ps, respectively. The corresponding 3 dB bandwidth is calculated to be 3.5 GHz (15 V), 3 GHz (10 V), and 2 GHz (3 V). The impulse response for future devices designed with abrupt junctions are shown in Fig. 5(d) with similar FWHM to the current devices. A considerably higher 3 dB bandwidth of 13 GHz(15 V), 11 GHz (10 V), and 10 GHz (3 V) due to smaller tail.

V. System Performance With and Without Equalization

The performance of an end-to-end optical link (Fig. 6) including the PD models derived in Fig. 5(c) and 5(d) has been evaluated using computer simulations. The optical link is comprised of a transmitter (T_x), Multi-Mode Fiber (MMF), and a Receiver (R_x) unit. The T_x block includes a random bit source (RBS), pulse shaping filter, 2-tap pre-emphasis feed-forward equalizer (FFE) and an MM-VCSEL. A train of 4000 random NRZ (Non-Return to Zero) is generated (by RBS) and convolved with pulse shaping low-pass filter with Tr = 12 ps (is 10–90% rise time) [21] and with MM-VCSEL with 3 dB bandwidth of 25 GHz. Both pulse shaping filter and VCSEL filter are modeled as Gaussian filters.

On the receiver (R_x) side, the VCSEL output is convolved with the impulse response of the Si PIN PD models at different biases (Fig. 5c and Fig. 5(d)). The output of the PD model is applied to a transimpedance amplifier (TIA) which is modeled as a third order Butterworth filter with a 3 dB bandwidth of 0.75$*$Bit Rate [22]. Further, a de-emphasis FFE was implemented in the optical link to overcome the channel bandwidth limits.

A. System Performance of the Fabricated Devices

The performance of the fabricated device (at 3 V, 10 V, and 15 V biases) in a full optical link (discussed above) was evaluated at the receiver output without equalizers.

Considering the PD model at 3 V bias the eye diagrams for 8 Gb/s with 0.47 eye-opening is shown in Fig. 7(a). Applying higher voltages effectively improves the vertical eye opening to 0.61 at 10 Gb/s (Fig. 7(b)) and 0.54 at 12.5 Gb/s (Fig. 7(c)) for 10 V and 15 V biases, respectively.

B. System Performance of Future Devices

Based on the measured PD characteristics and considering optimized epi-layer growth process that offers solution to minimize the extra tail effect on device bandwidth, the future Si PDs designed with abrupt junctions (see Fig. 5(d)) system performance is evaluated. Considering the future PD model at 3 V bias, the vertical eye opening of 0.96 at 10 Gb/s (Fig. 7(d)) and up to 0.68 eye-opening for 25 Gb/s are shown (Fig. 7(e)).

A set of 2-tap pre/de-emphasis FFEs are employed in both the transmitter and receiver ends to improve the signal quality. A pair of 2-tap pre-emphasis FFE is chosen in the way that the input pulse peak to the VCSEL driver is approximately equal to the original pulse peak without equalization [21], [23]. To obtain the maximum eye opening, a series of simulations are conducted to reach the optimum tap coefficients. For 50 Gb/s bit rate, using

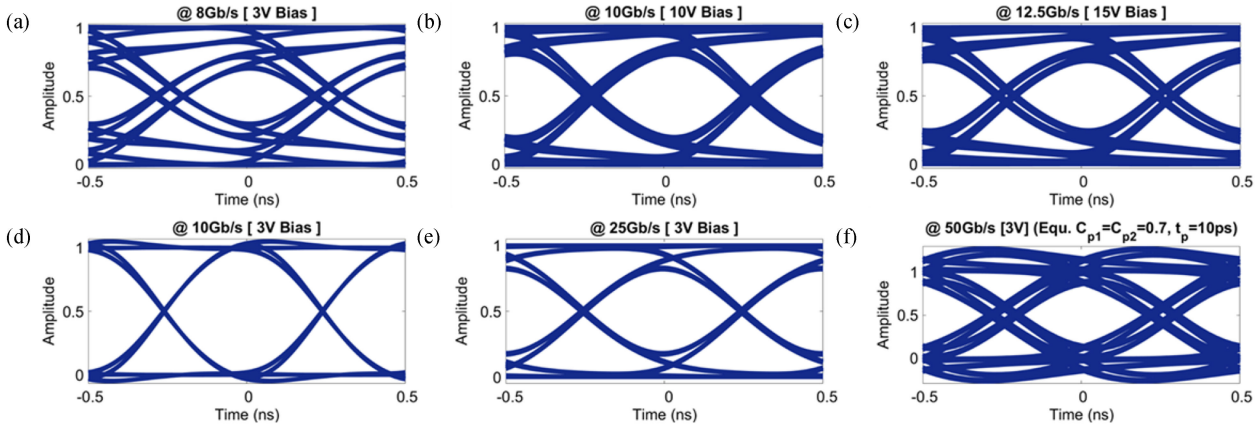

Fig. 7. Eye diagrams for an optical link with fabricated devices: (a) 8 Gb/s at 3 V bias, (b) 10 Gb/s at 10 V bias and (c) 12.5 Gb/s at 15 V bias. Eye diagrams for an optical link with future devices: (d) 10 Gb/s at 3 V bias, (e) 25 Gb/s at 3 V bias and (f) 50 Gb/s with 2-tap FFE at 3 V bias.

equal tap coefficients $(C_{p1} = C_{p2} = 0.7)$ the vertical opening of ∼0.7 (Fig. 7(f)) with $t_p = 10$ ps could be realized.

VI. Conclusion

A broadband CMOS-compatible surface illuminated silicon-based vertical PIN photodiode integrated with a photon trapping micro/nanoholes is demonstrated with more than 50% quantum efficiency at 850 nm. Employing measured optical and electrical characteristics of the fabricated devices with 30μm diameter into the PD model indicated deconvolved impulse response FWHM of ∼19 ps, ∼21 ps, and ∼23 ps at 15 V, 10 V, and 3 V biases. Implementation of scope and pulsed laser effect into the model combined with the tail extrapolation algorithm showed a strong agreement with the measured impulse response. Based on measurements and simulation results, fabricated devices can be operational at 12.5 Gb/s and future devices with optimum epi-material growth process can operate up to 25 Gb/s (NRZ) without equalization. Moreover, using an optimized 2-tap pre/de-emphasis FFE, future devices can reach up to 50 Gb/s.

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