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Maximizing Absorption in Photon-Trapping Ultrafast Silicon Photodetectors

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Silicon photodetectors (PDs) operating at near-IR wavelengths with high speed and high sensitivity are becoming critical for emerging applications, such as light detection and ranging (LIDAR) systems, quantum communications, and medical imaging. However, such PDs present a bandwidth-absorption trade-off at those wavelengths that have limited their implementation. Photon-trapping (PT) structures address this trade-off by enhancing the light–matter interactions, but maximizing their performance remains a challenge due to a multitude of factors influencing their design and fabrication. Herein, strategies to improve the PT effect while enhancing the speed of operation are investigated. By optimizing the design of PT structures and experimentally integrating them in high-speed PDs, a simultaneous broadband absorption efficiency enhancement up to 1000% and a capacitance reduction of more than 50% are achieved. Empirical equations correlate the quantum efficiency of PDs with the physical properties of the PT structures, material characteristics, and limitations of the fabrication technologies. The results that are obtained open routes toward designing cost-effective complementary metal–oxide-semiconductor (CMOS)-integrated receivers.

1. Introduction

Conventional silicon photodetectors (PDs) have weak absorption capabilities at near-IR (NIR) wavelengths, forcing them to be designed with thick absorbing layers to obtain high efficiency at the expense of limited speed of operation. Hence, the trade-off between speed and efficiency limits the use of Si, whereas other alternatives such as gallium arsenide (GaAs) are expensive and incompatible with complementary metal–oxide-semiconductor (CMOS) technologies. Considerable efforts have been devoted to enhance the efficiency and bandwidth simultaneously in Si-based PD to utilize the cost-effective and matured CMOS fabrication capabilities.[1–4] Detecting low levels of light at NIR at high speed is critical in emerging applications such as light detection and ranging (LIDAR), where a 3D image of the environment is required for virtual/augmented reality systems and robotics navigation systems.[5–8] PDs with high signal-to-noise ratio also allow building efficient optical communication systems,[9–11] whereas highly sensitive and fast PDs facilitate high-resolution biosensors, spectroscopy,[12] and medical imaging technologies.[13–15] In this effort, several photon-trapping (PT) structures,[4,16–23] which have been successfully implemented in solar cells, are now being implemented in PDs.[24–27] By introducing such PT structures on the surface, the reflection of light is reduced, and the optical path length is increased, enhancing the photon absorption and allowing the use of thinner semiconductor layers for faster carrier collection.[1,28] Using this approach, ultrafast and highly sensitive PDs have been demonstrated by several groups both for short[24,25,29–31] and longer wavelengths.[26,32–35] However, due to the different degrees of freedom for design and fabrication, the implementation of PT structures in PDs remains a challenge. Extensive design variations can be analyzed by numerical methods to optimize the performance of the device. This extensive exercise along with the uncertainties in the fabrication processes contributes to significant challenges in optimizing the device performance.

We conducted extensive simulation and designed vertical pin PDs with more than 150 unique-integrated PT structures by varying size, shape, period, and orientations, and established a crucial correlation between these parameters to enhance the device

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performances. Our rigorous simulations and extensive experimental investigations enabled a combination of optimum parameters to help to overcome the trade-off between speed and efficiency in the PDs, where the low absorption coefficient of silicon at NIR requires the use of a thick absorption layer, degrading its speed of operation. Besides, it allows high sensitivity for low levels of photon detection with 500% higher external quantum efficiency (EQE) as compared with the conventional PDs at 850 nm wavelength and up to 1000% enhancement at other NIR wavelengths around 1000 nm. In addition, our fabricated devices exhibit 35% reduction in junction capacitance due to the introduction of PT structures, with a potential for more than 50% reduction. This, in turn, improves the speed of operation. The extensive design variations make it the most comprehensive study aimed at understanding the PT phenomenon in high-performance PDs. To enable performance projections, it is of interest to develop simple, closed-form expressions for the EQE of the high-speed PT PDs that intuitively connect the physical parameters of the PT structures, material characteristics, and quality of fabrication. This work elucidates such crucial expressions to enable the implementation of the PT structures for absorption efficiency enhancement, capacitance reduction, and faster time response.

2. Results and Discussion

2.1. Device Design and Fabrication

The cross-sectional designs of mesa-type Si pin PDs with and without integrated PT structures are schematically shown in **Figure 1**a,b, respectively. The PDs consist of heavily doped p

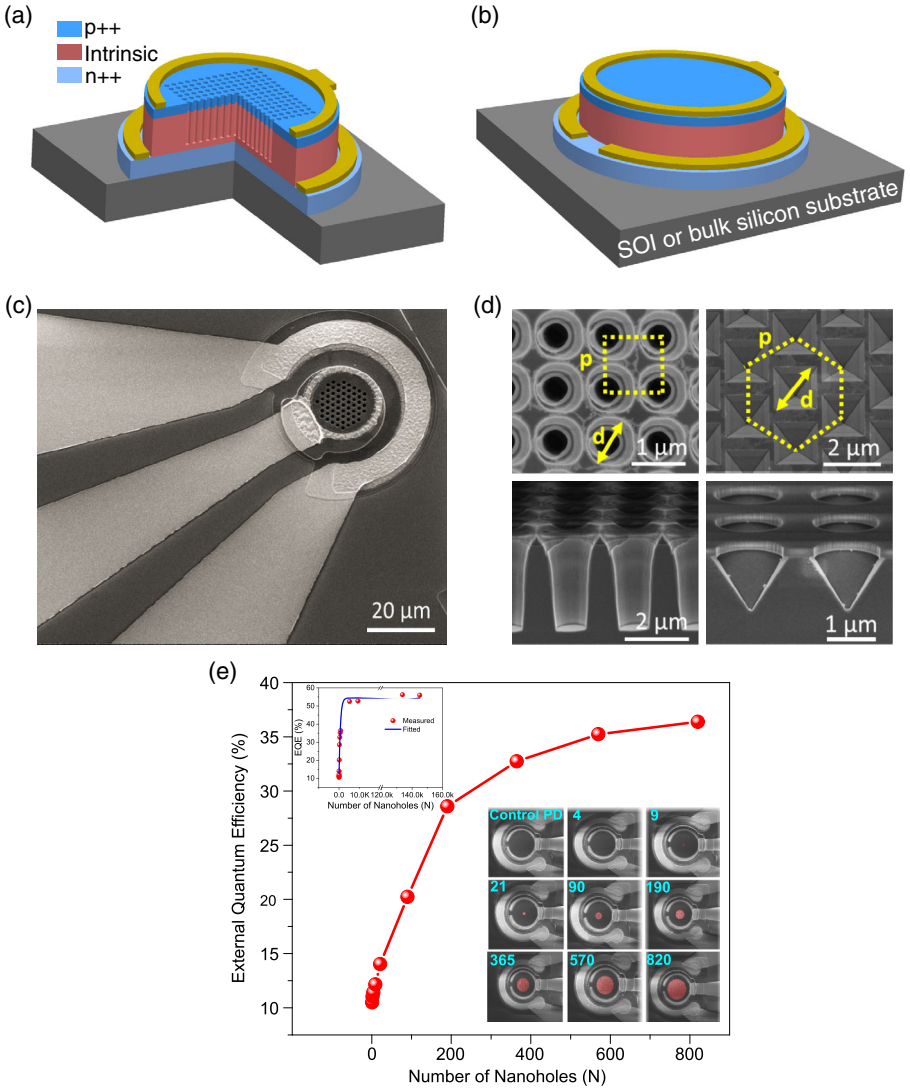

Figure 1. a) Schematic of Si pin PD with integrated PT structures for an *i*-layer of 2 µm thickness. b) A control PD without PT structures. Both devices are fabricated on SOI and bulk Si substrate. c) SEM image of PT PD with high-speed coplanar waveguide. d) Top and cross-sectional views of PT structures with funnel and inverted pyramid shapes for both square and hexagonal lattices. Over 40 different PT design variations in diameter, period, and shape are investigated. e) EQE versus number of nanoholes (*N*) in PDs under 850 nm laser illumination. Insets (top): fitted curve shows that EQE starts with ≈12% efficiency for control PD and saturates at ≈56% for PT PD with ≈5000 nanoholes. Inset (bottom): SEM images of PDs with an increasing *N* in devices with 50 µm diameter.

(p++)- and n (n++)-type Si layer and a 2 μm of thin intrinsic layer, epitaxially grown on the top of silicon on insulator (SOI) or bulk Si substrates. The PDs are fabricated with a different diameter (D) ranging from 30 to 500 μm. A SEM image of fabricated PD is shown in Figure 1c. An array of micro/nanoholes is patterned with a funnel shape or inverted pyramid etching profiles on the surface of the PDs, which serves as potential PT structures. These nanoholes are distributed in hexagonal or square lattices, designed with different diameters (d) and periods (p) ranging from 630 to 1500 nm and 900 to 3000 nm, respectively. Figure 1d represents the top and cross-sectional SEM images of PT holes with a tapered funnel and inverted pyramid shapes. The dimensions of the PT structures are selected to be close to the wavelengths of interest. The periodic distance between structures is reduced in each set of devices by keeping the d fixed, allowing to increase the number of nanoholes that can be accommodated on the surface of PD. The depth of the nanoholes was etched to be around 2 μm for funnel shape, whereas it varies between 450 and 1000 nm for inverted pyramids. Also, an unpatterned device is fabricated as a reference, which we call a control device to compare with the PT PDs (see Figure S1 and Table S1, Supporting Information, for more details on the investigated devices with the variation of different parameters, such as substrate, the diameter of PT holes, and periods).

2.2. External Quantum Efficiency

EQE is one of the key parameters that describes the sensitivity of PDs. Herein, several PT PDs with integrated nanoholes are designed, optically simulated, and fabricated, whereas the period, diameter, and number of nanoholes (N) are systematically varied. Using the following design guidelines, one can easily fabricate an optimized device by performing simulations beforehand. First, the influence of the N on the measured EQE is studied, where a set of devices with a constant device D of 50 μm is characterized. The SEM images of such devices with different values of N are shown in the inset of Figure 1e and Figure S2, Supporting Information. The measured EQE is presented in Figure 1e for PT PDs with a fixed period and a diameter of 1000 and 700 nm, respectively, for hexagonal lattice and inverted pyramid profile on SOI, where the value of N is varied from 0 (control) to 820. Compared with the control device with an EQE of ≈12%, the EQE of the PT devices gradually increases with increasing N, exhibiting a maximum of >38% for an N value exceeding 820. It is important to note that the test devices mentioned earlier were not among the designs with optimum parameters. This experiment mainly demonstrates a correlation between the EQE of a PD and N. Other periods and diameters that were optimized contributed to considerably higher peak efficiencies. The EQE enhancement observed in the device is due to the improved coupling of vertically incident light into laterally propagating modes with increasing N within the same area of the devices. Besides, a reduction of planar area in a device leads to decreased surface reflection and improved transmission of the incident light, resulting in relatively higher absorption in the photoactive layer. Consequently, the overall EQE of the PT devices is distinctly increased in comparison with the control device.

Next, the EQEs of 500 μm devices with higher N values and maximum up to 145 000 nanoholes with the same design as 50 μm diameter devices are added to establish a relationship, as shown in Figure 1e (top inset). It shows that, for this design with $d/p = 700/1000$, the EQE value can saturate at ≈56% for ≈5000 nanoholes. The maximum N presented in Figure 1e is 820 with a filling fraction ($\text{Area}_{\text{holes}}/\text{Area}_{\text{device}}$) of only 16% for the 50 μm device (see Figure S3, Supporting Information, for other filling fraction values), whereas a maximum of about 5000 nanoholes can be accommodated in the same device contributing to a very high filling fraction. Advanced foundry processes can accommodate almost 100% filling fraction by reducing the size of the features (such as contact electrodes, the separation between the region covered by the holes, and interconnect) using tighter fabrication tolerances.

Based on the fitting curve, an empirical equation can correlate the EQE of the devices with the PT structural and device parameters

$$\eta_{\text{PT}} = \eta_{\max}\Delta - a\Delta\left(\frac{p}{d}\right)[\exp(-bN)] \tag{1}$$

where η_{PT} is the EQE of a PT PD for a specific N, $\eta_{\max}$ is the maximum possible EQE (simulated value) for the device, a and b are the design constants, which were calculated to be 41 and 0.00147, respectively, for this design, and Δ is the ideality factor of the device. Δ represents the degrees of perfection in the fabrication process and material quality. When the value of Δ is 1, η_{PT} value gets closer to $\eta_{\max}$. Imperfection in device fabrication and the impurity of materials could lead to Δ smaller than unity, whereas in our devices, it varied between 0.75 and 0.81. Several of the η_{PT} values of fabricated devices are calculated based on Equation (1) with varying N, where a good agreement between the calculated values and the performances of the fabricated devices was observed (see Table S3, Supporting Information). Equation (1) is valid for any device diameter and can accommodate any number of nanoholes, as shown in the inset of Figure1e.

Next, the device is further optimized by varying the etching profile, d, p, and substrates (SOI and Si bulk substrate) to maximize the efficiency. The investigated PDs with 500 μm diameter have a filling fraction as high as ≈45%. The EQE of such PDs measured as a function of d/p is shown in **Figure 2**a, where the EQE values increase almost in a linear fashion as d/p changes from 0.4 to 0.8 due to the different 2D hole crystalline symmetries. The measured EQE reaches its maxima at $d/p = \approx 0.8$, which is due to the maximum influence of photon interaction with the 2D hole array, and, equivalently, the slowest photon velocity or the maximum PT, as shown in Figure S5, Supporting Information. The maximum EQE exhibited by the control device is about 15%, which is in good agreement with the finite-difference time-domain (FDTD) simulated control device. The PT PDs fabricated on a bulk Si wafer exhibit the EQEs between 15% and 25%. However, compared with the control and PT devices fabricated on bulk Si, the EQEs of PT PDs on SOI substrate distinctly increased, resulting in a very high EQE ranging between 30% and 56%. Subsequently, the influences of the etching profile of PT structures on the EQE are studied. The PT PDs fabricated on SOI substrate are arranged in hexagonal or square lattices with an inverted pyramid or funnel-shaped

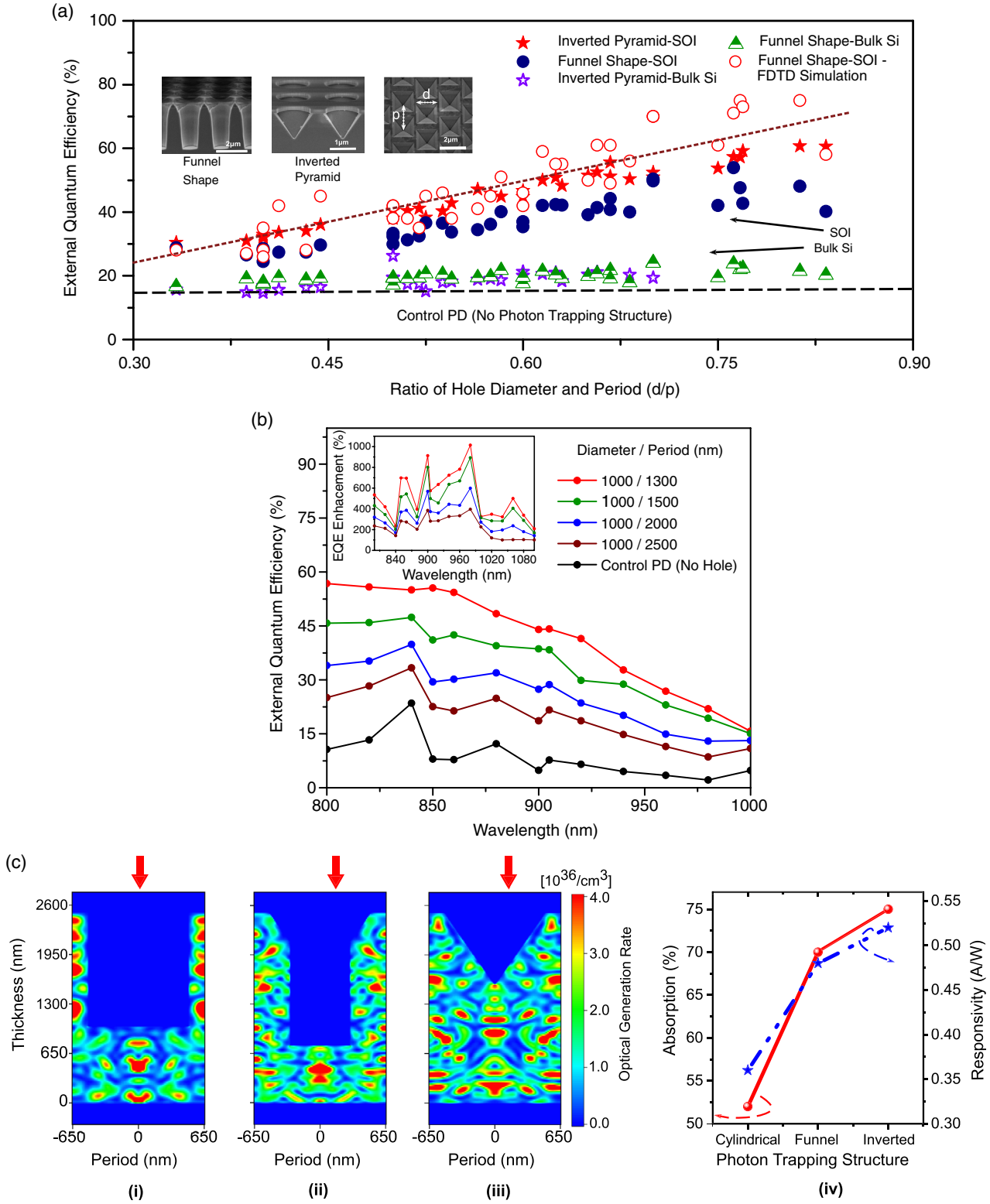

Figure 2. a) Experimentally measured EQE of fabricated Si PDs versus nanohole diameter/period for PT structures at 850 nm wavelength, whereas the PT structures (funnel shape and inverted pyramid) and substrate (bulk Si and SOI) were systematically varied. FDTD simulated EQE of a PD with funnel shape structure is also included (red hollow circle). Devices exhibit EQE from 15% to more than 60%. b) Broadband EQE enhancement in the fabricated PDs for wavelengths ranging from 800 to 1000 nm with a diameter of 1000 nm and decreasing periodicity. Inset: A 10× enhancement in EQE is observed at some wavelengths. c) Optical generation of carriers for different PT profiles: i) cylindrical, ii) funnel shape, and iii) inverted pyramid structures in Si PDs for a monochromatic wavelength of 850 nm. iv) Calculated maximum photon absorption and responsivity for such PT structures.

etching profiles. PDs with an inverted pyramid exhibit relatively higher EQE than the devices with a funnel shape. For instance, the inverted pyramid PDs with a d/p of 0.81 exhibit an EQE over 60%, whereas the EQEs exhibited by funnel shape are lower than 50% (see Figure S4, Supporting Information). This discernible enhancement obtained in the inverted pyramid can be attributed to the effective refractive index gradient in the interface of air and Si, resulting in a superior antireflection effect and efficient coupling of light over a wide wavelength and angular ranges.[36] This is an added advantage of PT structures over traditional quarter-wavelength thin-film antireflection coatings.[37]

The experimental results can lead to an empirical equation to capture the correlation between η_{PT} and the d/p in a very generalized fashion

$$\eta_{PT} = \eta_{flat} + \left(\frac{d}{p}\right)\Delta\beta \tag{2}$$

where η_{flat} is the EQE of the control devices, and β is the PT factor. β can be determined from the slope of a linear curve connecting multiple EQEs as a function of d/p. Equation (2) is valid for PD with both hexagonal and square lattices with varying β values, provided that a sufficient number of PT nanoholes are integrated on the surface of the PDs to reach saturation level in photon absorption (see Table S2, Supporting Information). Prior to fabrication, one can determine β by simulating a set of PDs as a function of d/p. The linear fitting curve drew using Equation (2) for the simulated funnel-shaped PDs is shown in Figure 2a. Several β values and η_{PT} for the simulated and fabricated devices are provided in Table S4 and S5, Supporting Information, and are found to be in good agreement with our observations. With a set of ideal simulations, one can estimate the efficiency of the fabricated devices as a function of d/p by following this design guideline.

Figure 2b shows the broadband measurements of 500 μm PDs incorporated with inverted pyramids in a hexagonal lattice formation. The wavelengths range from 800 to 1000 nm, whereas the nanohole p is varied by fixing the d to 1000 nm. Devices with a d of 1000 nm and a p of 1300 nm pronounce the highest EQE for all the incident wavelengths. This confirms that a high EQE can be attained for a relatively large d/p. In particular, the maximum efficiencies at the wavelengths of 800, 850, and 900 nm are measured as 58%, 56%, and 45%, respectively, for the PT devices with $d/p \approx 0.77$. The enhanced absorption coefficients at wavelengths, $\lambda = 800$, 850, and 900 nm, are calculated to be 4335.5, 4104.9, and 2989.2 cm^{-1} by assuming 2 μm of Si i-layer thickness, whereas the absorption coefficients for bulk Si at those λ points are 850, 535, and 306 cm^{-1}, respectively. Hence, a maximum of about >10 times higher absorption enhancement is attained at some of the incident wavelengths by integrating inverted pyramids or funnel-shaped nanoholes in the PDs fabricated on SOI substrates (Figure 2b, inset). Herein, the SiO_2 layer of the SOI substrate acts as a mirror due to the high refractive index difference between Si and SiO_2, resulting in an enhanced reflection and, consequently, a higher absorption in the i-layer of the PDs. Furthermore, the optics of the PDs with such PT structures are simulated, obtaining the optical generation rate for a wavelength of 850 nm, as shown in Figure 2c. PD with a cylindrical-shaped structure is also presented as a comparison. A higher number of modes are seen in (iii) inverted pyramid nanohole devices as compared with (i) cylindrical- and (ii) funnel-shaped nanohole devices due to the reflection at the interface of SiO_2 and Si and enhanced lateral propagation of incident light within the devices. Hence, inverted pyramid PDs fabricated on SOI substrates noticeably exhibit higher absorption in comparison with the PDs fabricated on bulk Si and SOI substrates. The simulated inverted pyramid structures exhibit 75% and 0.53 A W^{-1} absorption efficiency and responsivity, respectively, whereas the PDs with etching profiles of the funnel and cylindrical shapes exhibit the absorption efficiencies of 70% and 52% and the responsivities of 0.49 and 0.36 A W^{-1}, respectively (Figure 2c-iv and Figure S6, Supporting Information).

2.3. Capacitance Reduction

In junction PDs, the 3 dB bandwidth is dependent on two parameters: the carrier transit time (t_r) and the RC constant time.[38] A reduction in the junction capacitance due to the presence of the PT nanoholes can be considered to write the following modified expression of f_{3dB}.

$$f_{3dB} = \frac{1}{\sqrt{[2\pi RC(1-ff)]^2 + [t_r/0.44]^2}} \tag{3}$$

where t_r is the transit time required for the carriers to reach the electrode at saturation velocity, R is assumed as 50 Ω, and ff is the filling fraction of the nanohole array (see Figure S8, Supporting Information). By considering the pin PD as a parallel plate, the capacitance can be written as $C = \varepsilon_o\varepsilon_r A/w$, where ε_o and ε_r are the permittivity of vacuum and silicon, respectively; w is the depletion layer width, typically the i-layer, and A is the junction area. The integration of an array of PT holes leads to the reduction of effective cross-sectional area and active materials in the PDs. Consequently, the overall junction capacitance of a PD is reduced proportionally to the ff of the nanohole array. The use of a thin i-layer in conventional PDs reduces the transit time but increases the junction capacitance. Such a trade-off is effectively addressed with integrated PT nanoholes.

Figures 3a,b shows the results of capacitance–voltage (C–V) measurements performed on the PDs with a diameter of 30 and 80 μm, respectively. The top-left insets represent the top view of SEM images of PDs. The experimental C–V measurements between the control and the PT PD show a 15% and 35% of capacitance reduction for PDs with 30 and 80 μm of diameter, respectively. Such reduction is corroborated by applying analytical modeling of the capacitance based on the doping profile and built-in potential as described in Equation (S3), Supporting Information, and other references.[39] Furthermore, the same investigation is also conducted for devices with 40 and 50 μm diameter and included in Figure S7, Supporting Information. Higher capacitance reduction is observed as the diameter of the PDs increases, because, in our current design, a larger diameter of PD allows to accommodate a higher number of nanoholes. Both devices can reach >50% (see Figure S9, Supporting Information) of capacitance reduction by decreasing the area occupied by the ohmic contacts on the surface of the PDs using CMOS foundries where the width of metal contacts can be less than 150 nm.[40]

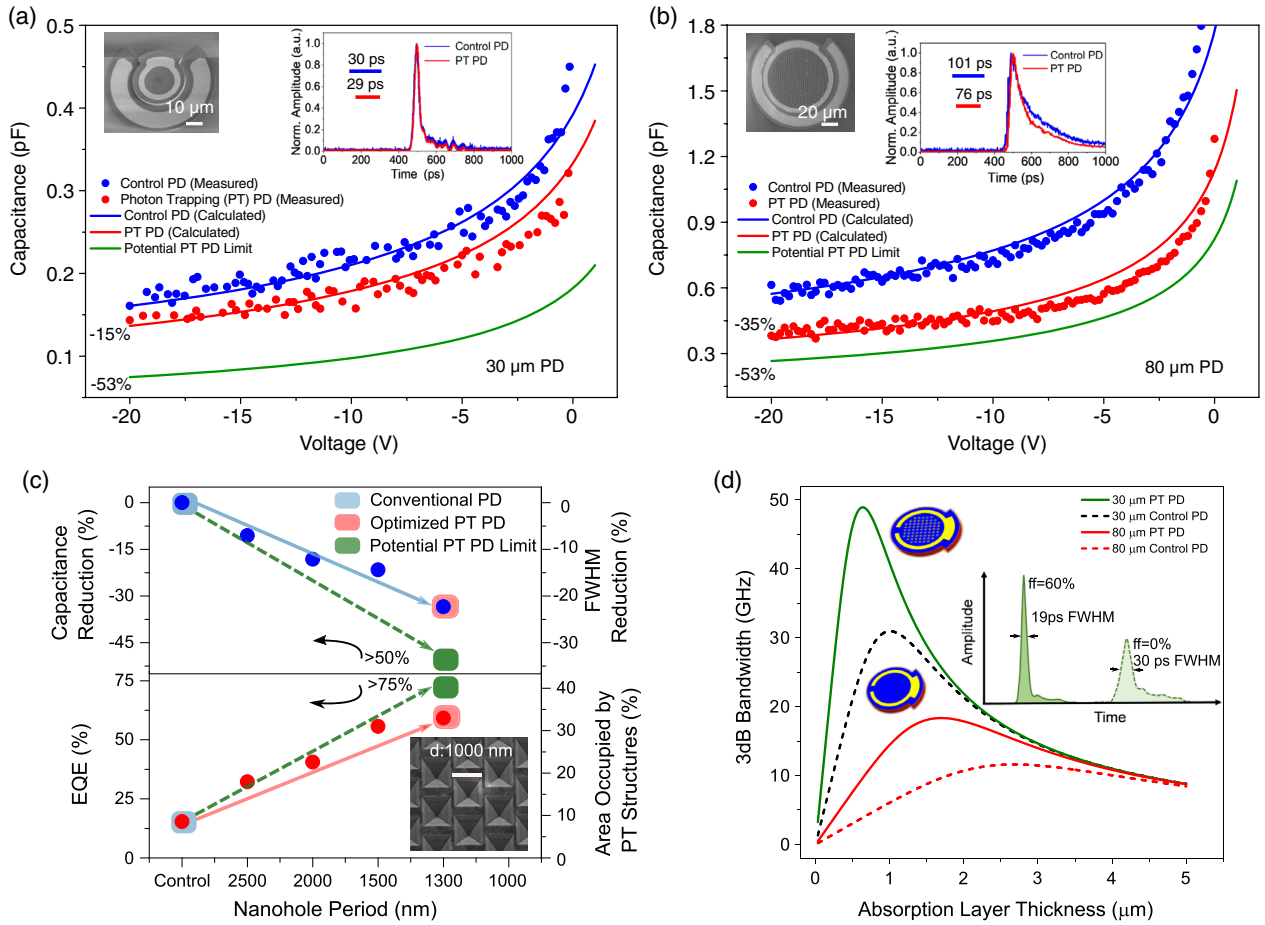

Figure 3. Capacitance–voltage characteristics of PDs comparing PT and control device with a) 30 and b) 80 μm diameters, confirming a 15% and 35% capacitance reduction, respectively. This leads to up to 25% narrower FHWM in the pulse time response (inset). Over 50% capacitance reduction can be realized by increasing the number of PT nanoholes. c) A study of >150 different devices are used to optimize PT PDs with simultaneous improvement in EQE, reduction in capacitance, and enhancement in time response. A set of devices with a fixed *d* of 1000 nm and different periods are used to show that >50% of capacitance reduction and >75% of EQE can be achieved at 850 nm. d) Modeling of 3 dB bandwidth versus absorption layer thickness considering 60% of capacitance reduction in PT PDs. Illustrations in the inset show a stronger signal amplitude, and a narrower impulse response of 19 ps is possible in a 30 μm PT PD shown in (a).

The impulse responses of the fabricated PDs are measured under 850 nm illumination and shown in the insets of Figure 3a,b. The full-width-half-maximum (FWHM) of the impulse response has been reduced up to 25% in the PD with 80 μm diameter. This is due to the reduced effective capacitance and consequently reduced *RC* time in PT PDs compared with the control devices. Higher FWHM and *RC* time reduction can be achieved in optimally designed PT PDs by fabricating them with closely packed nanoholes and narrower ohmic contacts in advanced semiconductor foundries. The impulse responses of control and PT PDs with larger diameters of 40 and 50 μm are presented in Figure S7, Supporting Information. The collective absorption enhancement of >75%, the capacitance reduction of >50%, and the FWHM reduction of >35% shown in Figure 3c and Figure S9, Supporting Information, allow any designer to optimize the PDs with integrated PT structures. Figure 3d shows how a drastic reduction in the capacitance can dramatically enhance the ultrafast operation of a PD. For example, the impulse response of our control device with 30 μm of diameter is measured to be 30 ps, and with optimum PT nanoholes, it can exhibit ≈19 ps FWHM (Figure 3d, inset).

3. Conclusion

Through extensive simulations and experimental implementations of PT structures in silicon PDs, we helped divulge a direct correlation between the enhancement of absorption and physical parameters of the PT structures integrated in the PDs. We used cylindrical nanoholes, inverted pyramids, and funnel-shaped surface formations and achieved up to 1000% higher quantum efficiency compared with the control devices. This was made possible by bending the incident beam of light and enabling lateral propagation of modes to prolong the light–matter interactions and suppress back reflection. The enhancement in absorption also comes with a considerable reduction in device capacitance by more than 35% and, thereby, an improvement in the time response. The combined effect collectively can help

to overcome the trade-off between the efficiency and the speed of operation of the PDs. State-of-the-art CMOS fabrication processes could enable near-perfect EQE and above 50% capacitance reduction, by increasing the number of PT nanoholes integrated into the devices, especially in photodiodes with small surface area, required to operate at high speed (Figure 3c and Figure S8, Supporting Information). Analytic equations based on empirical modeling are presented to make it possible to correlate, with high accuracy, the PT efficiency of the PD with physical properties of the PT structures, material characteristics, and limitations of the fabrication technologies. Such results open opportunities for the development of complete CMOS-integrated receivers operating with high sensitivity and high speed and can be expanded to other semiconductors, such as germanium (Ge), gallium arsenide (GaAs), and indium phosphide (InP)-based ternary and quaternary materials.

4. Experimental Section

Fabrication of PT PDs: Mesa-type Si pin PDs are fabricated with a total thickness of 2.5 μm. Heavily doped regions of p and n exhibit reduced electron and hole lifetime of carriers, respectively, facilitating relatively lower diffusion of photogenerated carriers into the high-field *i*-layer region. In addition, it reduces the series resistance. The fabrication processes were done in class 100 cleanroom. The PIN wafers on bulk Si or SOI were cleaned in a piranha solution (10:1) to remove organic residues. For inverted pyramids nanoholes, 200 nm of silicon nitride was deposited by plasma-enhanced chemical vapor deposition at (PECVD) 250 °C and serves as a masking layer for potassium hydroxide (KOH) etching. Next, deep ultra violet (DUV) lithography was used to pattern the nanoholes on the wafer followed by deep reactive-ion etching (DRIE) etching to pattern the silicon nitride. KOH etching was performed with a solution at 33% for 2:30 min at 65 °C. Next, DRIE was used to reach the n-mesa and p-mesa of the device, allowing to deposit by evaporation 100 nm of Al and 200 nm of Pt that serves as the n-ohmic and p-ohmic contacts. Finally, the wafers were treatment with hydrofluoric acid for 10 s to minimize the leakage current. The fabrication of photon trapping structures with a funnel etching profile[41] and other passivation methods[42] can be found in other references.

Optical Simulation Method: The FDTD optical wave propagation simulation method is used to calculate the electromagnetic field distribution within PD. In this simulation, a plane wave with a wavelength of 850 nm is a normal incident to the surface of a PD. Periodic boundary conditions (PBC) are assumed laterally between unit cells, and perfect matching layer (PML) boundary conditions are set at the top and bottom of the Si PD. In the first step, the photon absorption is calculated, where electromagnetic field distributions are used as input parameters. The absorption (*A*) is obtained from the subtraction of the transmission (*T*) and the reflection (*R*) as $A = 1–T–R$. In the next, the EQE, which is defined as the ratio of the total incident power on the PD to the amount of photon absorbed in the intrinsic layer, is calculated, whereas it is assumed that all the photogenerated carriers are collected by the electrodes. Finally, the current density is calculated from the quantum efficiency.

Pulse Time Response Measurements: A mode-locked pulsed laser with a sub-picosecond pulse width is used, where the PDs are illuminated by an 850 nm wavelength with a biasing over 3 V bias. The generated electric pulses are delivered to a 20 GHz sampling oscilloscope via a ground-signal-ground (GSG) probe and 25 GHz bias-T.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

absorption, photodetectors, photon trapping, silicon, ultrafast operation

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